PLESSEY
SEMICONDUCTORS

Radio Communications Handbook

Radio Communications Handbook

James M. Bryant, Applications Manager, Radio Communications Group.

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Foreword

Plessey Semiconductors originally developed the SL600 series for use in military SSB systems. For such applications, hermetic packages and full-temperature operation are necessary: the SL600 series devices meet such specifications. As the range expanded, requirements arose for less expensive versions of SL600 devices and the SL1600 series was introduced. The SL1600 series consists of the same chips as are used in the SL600 series but packaged in plastic DIL packages (mostly 8-lead minidips) tested to less stringent specifications, and supplied with a —30°C to +70°C temperature specification. In a few cases some of the pins present in the SL600 devices are omitted in the SL1600 devices in order to allow a chip previously supplied in a 10-lead TO-5 to be encapsulated in an 8-lead minidip.

SL600 and SL1600 type numbers are used in section headings but to avoid tedious repetition, only the SL600 type numbers will be used in the text unless there are significant differences between the SL600 and SL1600 devices. Pin numbers generally refer to both types; in cases where pin numbers differ, the pin numbers for the SL1600 device is given in brackets, e.g. Pin 6(7).

Not all SL600 devices have corresponding SL1600 types and there are one or two SL1600 devices which do not have SL600 counterparts. Where this occurs the text will make clear which types are available. If, however, there are two devices having the same two final digits (e.g. SL1610 and SL610), then they will always be the same chip and function.

J.M.B.

Section 1
Circuit details

SL610C, SL611C, SL612C, SL1610C, SL1611C & SL1612C

RF/IF amplifiers

The SL610C, SL611C and SL612C integrated RF amplifiers are similar circuits, having typical voltage gains of 10, 20 and 50 and upper 3dB gain points at 140MHz, 100MHz and 15MHz respectively. The first two draw a supply current of about 15mA at 6V and have some 50dB AGC range while the SL612C draws 3.5mA and has 70dB of AGC. All three are intended to use with +6V supplies and have internal decoupling. They will drive an output signal of about 1V rms.

The cross-modulation of the circuits is 40dB down on signal at 1V rms output with no AGC, and at 250mV rms input with full AGC. The input and output admittances of the circuits are not greatly affected by AGC level.

CIRCUIT APPLICATIONS

There are seven connections to each circuit: an input, an input bias point, an AGC input, the output, the positive supply pin and two earths — for input and output respectively.

The positive supply should be 6V, but the devices will function at supplies of up to 9V. Since internal HF supply decoupling is incorporated a certain amount of HF ripple can be tolerated in the supply. LF ripple should be kept down as it can cause intermodulation — especially at large HF signal levels — and 10mV rms of LF ripple should be considered a maximum.

The AGC characteristic is shown in Fig. 1. It is temperature dependent, so that while a potentiometer may be used to provide a gain control voltage the gain so defined will not be temperature stable to better than ± 2dB. The AGC terminal will normally draw about 200 microamps at 5V — in some SL610C and SL611C devices this may be as high as 600 microamps.

There are two earth connections: pin 4 is the input earth and pin 8 the output earth. When several devices are cascaded pin 8 of one stage and pin 4 of the next should have a common earth point — also high common earth impedances to pin 4 and pin 8 of the same device should be avoided. Fig. 2a shows a circuit where common earth impedance could cause instability and Fig. 2b shows one where the input and output signals have correct point earthing. If extra supply decoupling is used the capacitor should ground to the output earth point. The can should be separately earthed in applications at VHF or in the presence of a large RF field.

The input bias point (pin 6) is normally connected directly to the input (pin 5) and the signal applied through a capacitor but occasionally, when the signal is obtained from a tap on a coil, the arrangement in Fig. 2b may be used to give slightly improved noise performance. C_D is a decoupling capacitor. The SL610/611 noise figure is approximately 4dB at 300 ohms source impedance and 6dB at 50 ohms and at 2.5 kilohms, the noise figure for the SL612 is 3dB at 800 ohms source impedance.

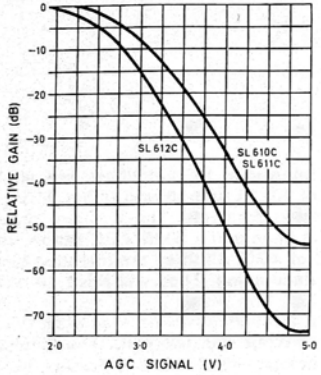


Fig. 1 SL610/11/12 AGC characteristics

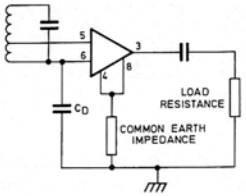
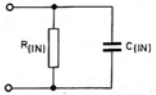


Fig. 2(a) Incorrect connections of earths



(a) input circuit

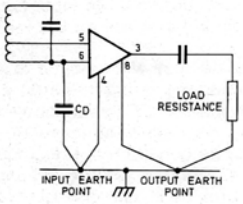
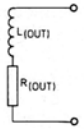


Fig. 2(b) Correct connection of earths



(b) Output circuit

Fig. 3 Equivalent circuits

Both the input admittance G_{11} and the output impedance G_{22} have negative real parts at certain frequencies. The equivalent circuits of input and output respectively are shown in Figs. 3a and 3b and the values of R_{in}, R_{out}, C_{in} and L_{out} may be determined for any particular frequency from the graphs Figs. 4 and 5. It will be seen that for the SL610C and the SL611C, R_{in} is negative between 30 and 100MHz, and R_{out} is negative over the whole operating frequency range. For the SL612C, R_{in} is not negative and R_{out} is negative only below 700kHz.

If an inductive element having inductance L1 and parallel resistance R1 is connected across the input, oscillation will occur if R_{in} is negative at the resonant frequency of C_{in} and L1, and if R1 is higher than R_{in}. Similarly, if a capacitor C1 in series with a resistance R2 is connected across the output oscillation will occur if, at the resonant frequency of L_{out} and C1, R_{out}, has a negative resistance greater than the positive resistance R2. Where the input is inductive, therefore, it may be shunted by a 1k resistor; where the load is capacitive, 47 ohms should be placed in series with the output.

Suitable input arrangements for the amplifiers are shown in Fig. 2b and Fig. 6. The method shown in Fig. 6a is representative of all inputs — the input and bias points are directly-connected and the signal is coupled via a capacitor. If the input is inductive the 1k resistor shown in Fig. 6b may be required, although usually it can be omitted. If a crystal filter is used it should be correctly terminated, allowing for the impedance of the IC, and coupling made via a capacitor.

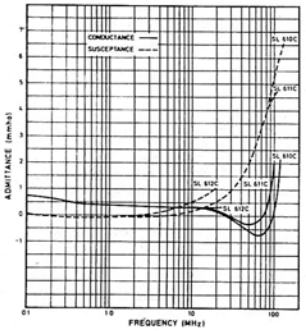


Fig. 4 Input admittance with o/c output (G_{11})

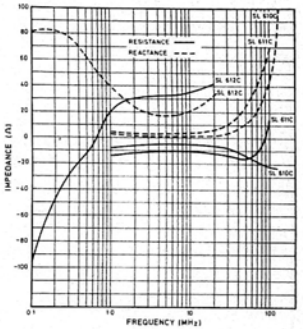
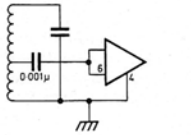
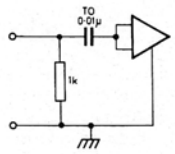


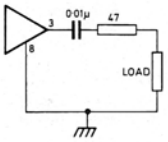
Fig. 5 Output impedance with s/c input (G_{22})



(a) Tuned circuit



(b) Normal input circuit



(c) Normal output circuit

(d) Current drive into inductance

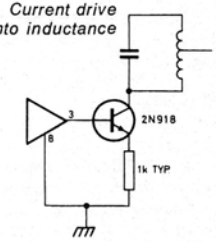
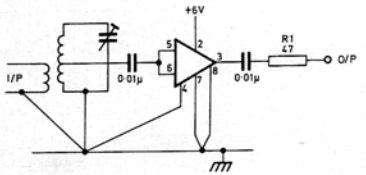
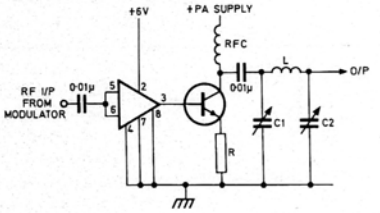


Fig. 6 Input and output circuits

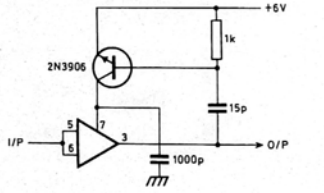
The output is a voltage source, with the impedance characteristics mentioned above. Output coupling is via a capacitor, with a series resistor if necessary to preserve stability (Fig. 6c). If a current output to a tuned circuit is required the arrangement in Fig. 6d is suitable, using almost any small signal NPN transistor with an f_T of over 300MHz and low C_{OB}. To drive particularly low impedances, e.g. a 50 ohm coaxial cable, this impedance should be increased somewhat by a series output resistor (say, 100 ohms) as, if the output is loaded directly by low impedance, most of the negative feedback will be removed — with consequently poor linearity and constancy of gain. Examples of the use of these amplifiers are shown in Fig. 7.



(a) *RF preamplifier. Use SL610C up to 140MHz, SL611C up to 70MHz, SL612C up to 12MHz. R1 may be omitted if the load is neither capacitive nor very low impedance.*



(b) *Linear power amplifier for low power SSB transceivers. L, C1 and C2 form the output π tank circuit. The values of PA supply and R should be chosen to suit the transistor used. C_{ob} should be as low as possible.*



(c) *Constant level RF amplifier stabilising at approximately 500mV rms output over a range of inputs greater than 20dB. SL610C, 611C or 612C may be used. With tuned feedback, this circuit makes an excellent constant level oscillator.*

Fig. 7 SL610/11/12

SL613C & SL1613C

Limiting RF amplifier/detectors

The SL613C is a simple but versatile circuit consisting of a broadband amplifier with excellent limiting characteristics, and a simple transistor detector. The broadband amplifier has 3dB points of 5 and 150 MHz, a 4.5dB noise figure, and a gain of 4. The detector starts operating with an input of about 10mV rms and limits, with the main amplifier, at 120mV rms input, when the detected output current is about 1mA. The circuit, which has internal bias and supply decoupling, consumes 15mA at 6V supply.

CIRCUIT DESCRIPTION

The circuit diagram of the SL613 is given in Fig. 8. The limiting amplifier consists of the long-tailed pair of transistors, TR1 and TR2, the output of which drives an emitter follower output stage, the detector and the other input of the long-tailed pair via a potential divider to provide negative feedback, The potential divider defines the gain of 4, and the 330pF DC blocking capacitor defines the low frequency 3dB point of 5 MHz. Careful design of both the long-tailed pair and the bias and feedback circuitry ensure that the amplifier limits symmetrically.

The detector consists of TR4 and TR5 (a matched pair) and the output current appears on the collector of TR5. There is a small leakage current of about 30 microamps with no signal input.

CIRCUIT APPLICATIONS

Fig. 9a shows the SL613C used as an amplifier and detector. Only two capacitors and a resistor are used, pins 1 and 8 are connected together internally to the case of the device and to the output earth. If possible both should also be connected together externally to minimise lead inductance. Pin 5 is the input earth. The rules concerning the input and output earths of the SL610/11/12 apply equally to the SL613C. Power is connected to pin 2 and should be between +6V and +7.5V and free of LF ripple; small amounts of HF ripple will be removed by the internal HF decoupling.

Pin 3 is the RF output and has an output impedance of about 35 ohms and 3pF. It must always be isolated at DC by a capacitor and should not be required to drive a capacitive load of over 10pF, or a resistive load of under 50 ohms, without a buffer resistor of about 50 ohms. While instability is unlikely if this precaution is neglected, it is possible and in any case the response of the SL613C is severely affected.

The detected output on pin 4 is a current flowing out of a transistor collector. The pin must always be biased between +3V and +9V, even if the detector output is not used. In this latter case pins 2 and 4 are generally connected together. There is normally a small leakage of some 30 microamps with no signal, which rises quite linearly to 1mA at 120mV rms input, at which point the amplifier limits and the detected output no longer increases with signal input. This detector was designed as an AGC detector but may be used quite successfully as an AM envelope detector provided that the signal is not more than 90% modulated and does not limit the amplifier on positive peaks.

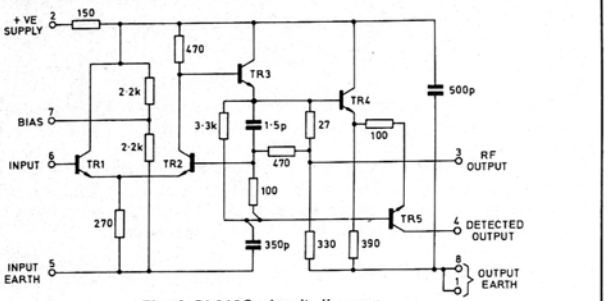


Fig. 8 SL613C circuit diagram

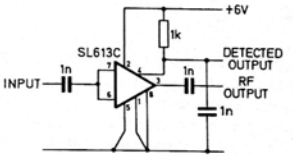
Pin 6 is the signal input. It is normally connected directly to the bias pin, pin 7, but may be used, like the SL610/11/12 input pin, in the circuit shown in Fig. 2b, i.e. with pin 7 connected to the 'cold' end of a coil and decoupled to earth and pin 6 connected to the 'hot' end of the coil. The impedance of the input pin alone is 5 kilohms and 6pF but if it is connected to pin 7 this falls to 800 ohms and 8pF. Inputs of over 1.5V rms will overload the limiting amplifier and should be avoided.

The gain from pin 6 to pin 3 is 4 (12dB) and the noise figure, with a source impedance of 500 ohms is 4.5dB. The amplifier limits when the input exceeds 120mV rms.

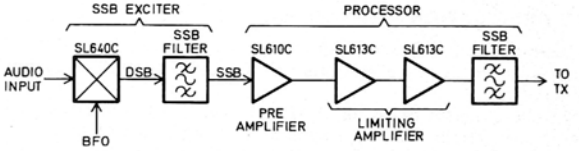
Typical uses of the SL613 are shown in Figs 9b and 9c. They consist of a speech processor for SSB transmitters which can increase the average/peak power ratio by up to 12dB and an auxiliary AGC system for AM receivers using a SL621 speech AGC system.

The SSB processor in Fig. 9b consists of two SL613C's, an SL610C and a SSB filter. An SSB signal is produced in one of the usual ways (in this case by the filter method), amplified by the SL610C and fed to two cascaded SL613C's. These clip the signal but, because of their excellent symmetry, preserve the zero-crossing points. The resulting signal consists of the required clipped SSB signal together with harmonics and intermodulation products which are removed in a SSB filter, leaving only the clipped SSB which is then transmitted. This system has little effect on intellegibility (although it alters voices somewhat) and improves the mean/peak power ratio of a normal SSB signal by up to 12dB. A danger of adding such a system to an existing SSB transmitter is that the increased power may cause damage to inadequately designed linear amplifiers, but if this is not a problem the increase in effective power for the same amplifier power is well worth the cost of the extra filter and integrated circuits.

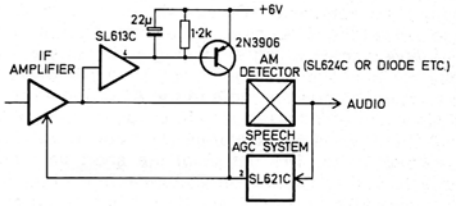
The carrier AGC system in Fig. 9c is normally inoperative since a small modulated signal will supply the SL621C with sufficient audio to maintain AGC. If the modulation is removed the SL621C will provide no AGC and the carrier level rises until the detected current in the SL613C turns on the PNP transistor (a 2N3906 is shown but any small Si PNP type will suffice) and provides AGC again, preventing the IF amplifier from limiting.



(a) *An amplifier/detector*



(b) *Signal processors for SSB transmitters*



(c) *Supplementary carrier AGC system for AM receivers using SL621C speech AGC*

Fig. 9 SL613C application

SL620C, SL621C, SL1620C & SL1621C

AGC generators

The SL621C is an audio-operated AGC generator designed for use with the SL610/11/12 RF amplifiers in SSB receivers. The SL620C, designed to provide AGC to the SL630C audio amplifier, is exactly similar in operation to the SL621C and is, therefore, not separately described in this section.

An ideal single sideband AGC generator must set the AGC rapidly when a new signal appears and follow a rising or fading signal but, if the signal disappears altogether (as in pauses in speech), retain the AGC level until the signal recommences. If the signal remains absent for more than a preset time, however, the system should rapidly revert to full gain. The SL621C will perform these functions and will also produce short-lived pulses of AGC to suppress noise bursts.

CIRCUIT DESCRIPTION

The operation of the circuit is described with reference to Fig. 10, which also illustrates the dynamic response of a system controlled by an SL621C AGC generator.

The SL621C consists of an input AF amplifier, TR1-TR4, coupled to a DC output amplifier, TR16-TR19, by means of a voltage back-off circuit, TR5, and two detectors, TR14 and TR15, having short and long rise and fall time constants respectively.

An audio signal applied to the input rapidly establishes an AGC level, via TR14, in time t_1. Meanwhile the long time constant detector output (TR15) will rise and after t_3 will control the output because this detector is the more sensitive. If the signals at the SL621C input are greater than approximately 4mV rms they will actuated the trigger circuits TR6-TR8 whose output pulses will provide a discharge current for C2 via TR10, TR13.

By this means the voltage on C2 can decay at a maximum rate which corresponds to a rise in receiver gain of 20dB/sec. Therefore the AGC system will smoothly follow signals which are fading at this rate or slower. However, should the receiver input signals fade faster than this, or disappear completely as in pauses in speech, then the input to the AGC generator will drop below the 4mV rms threshold and the trigger will cease to operate. As C2 then has no discharge path, it will hold its charge (and hence the output AGC level) at the last attained value. The output of the short time constant detector (TR14) falls to zero in time t_2 after the disappearance of the signal.

The trigger pulses also charge C3 via TR9, thus holding off TR12 via TR11. When the pulses cease, C3 discharges and after t_5 turns on TR12, rapidly discharging C2 (in time t_4) thus restoring full receiver gain. The hold time, t_5, is approximately one second with C3=100 microfarads. If signals reappear during t_5, then C3 will re-charge and normal operation will continue. The C3 re-charge time is made long enough to prevent prolongation of the hold time by noise pulses. Fig. 10 also shows how a noise burst superimposed on speech will initiate rapid AGC action via the short time constant detector while the long time constant detector effectively remembers the pre-noise AGC level.

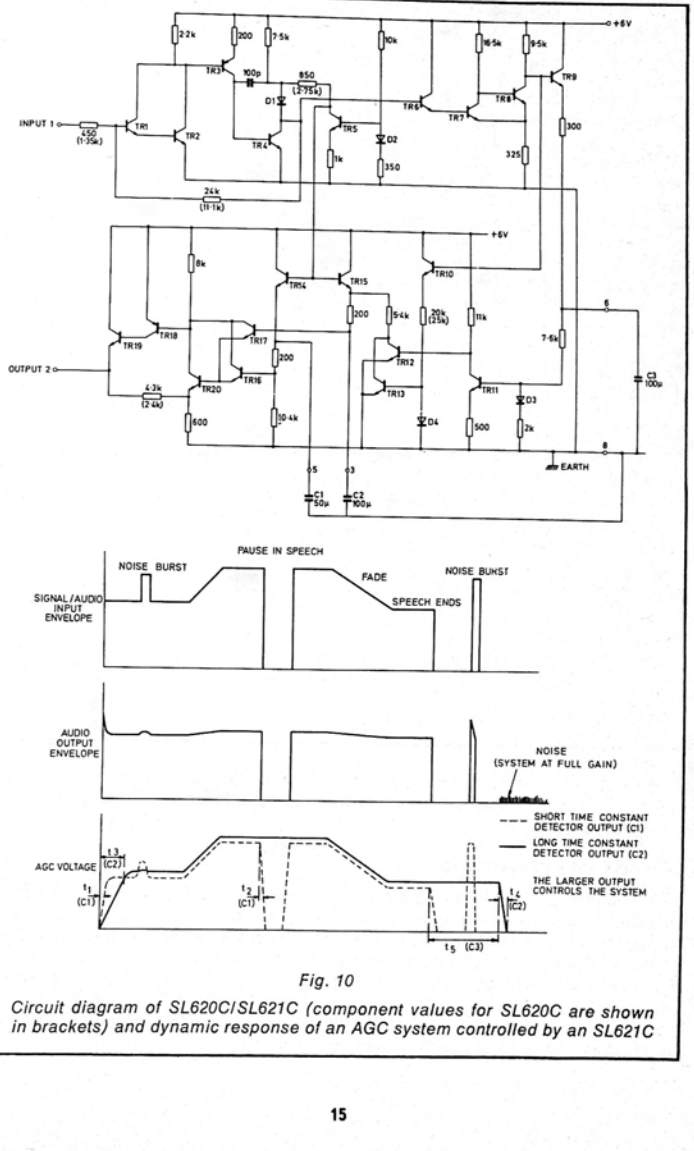


Fig. 10

Circuit diagram of SL620C/SL621C (component values for SL620C are shown in brackets) and dynamic response of an AGC system controlled by an SL621C

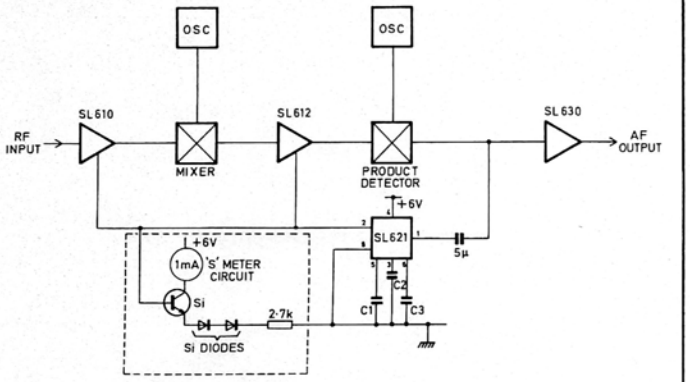


Fig. 11 An SL621C used to control an SSB receiver

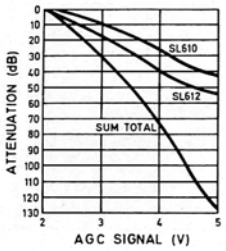


Fig. 12 Attenuation v. AGC signal

The various time constants quoted are for C1=50 microfarads and C2=C3=100 microfarads. These time constants may be altered by varying the appropriate capacitors.

CIRCUIT APPLICATIONS

The SL621 is used in an SSB receiver as shown in Fig. 11. AGC need only be applied to two of the gain stages even if there are more than two such stages in the receiver since AGC applied to two stages only will result in over 120dB AGC range. It is usual to apply AGC to the first RF stage and the first IF stage and it will be seen from Fig. 12 that an SL612 IF amplifier reacts earlier to an increasing AGC voltage than an SL610C RF amplifier. This has the effect of delaying the AGC to the input stage, thus improving the receiver signal to noise ratio at low AGC levels.

Fig. 12 also shows the total attenuation to be expected at any AGC voltage when AGC is applied to one SL610C and one SL612C in a system; from this one can calculate the calibration of an 'S' meter for use with the SL621C. Such a meter, as shown in Fig. 11, should have a sensitivity of 2.6V FSD and be calibrated linearly from 0 to 120dB.

The output current capability of the SL621 is not high and it should not be expected to drive more than three SL610/11/12 devices in addition to an 'S' meter circuit similar to that shown in Fig. 11.

There are two other important points to observe when using the SL621C: supply de-coupling and input coupling. Since capacitors C1 and C3 may need to charge very quickly, the source impedance of the 6V supply line at low frequencies should be very low, if necessary being decoupled by a low impedance 1000 microfarad capacitor placed near the SL621C.

The input should be applied to pin 1 via a capacitor of not more than 470 ohms reactance at the lowest input frequency encountered, and should never exceed 1Vrms. Input voltages in excess of this level may cause the internal amplifier to block, with consequent failure of the AGC voltage. The condition can be avoided, if necessary, by using a diode limiter at the input. However, the problem hardly ever arises with the SL621 (which has a threshold of about 8mV) but is more common with the SL620 (which has a threshold ten times greater).

In the presence of RF fields the AGC line may need to be decoupled: a 5000pF capacitor from pin 7 of each RF amplifier to earth and a 100 ohm resistor from each pin 7 to the AGC line should be adequate. It is, however, important not to use a capacitance greater than 15000pF, otherwise the impulse suppression characteristic of the circuit will be degraded.

The SL621 may be used with supply voltages between +6V and +9V.

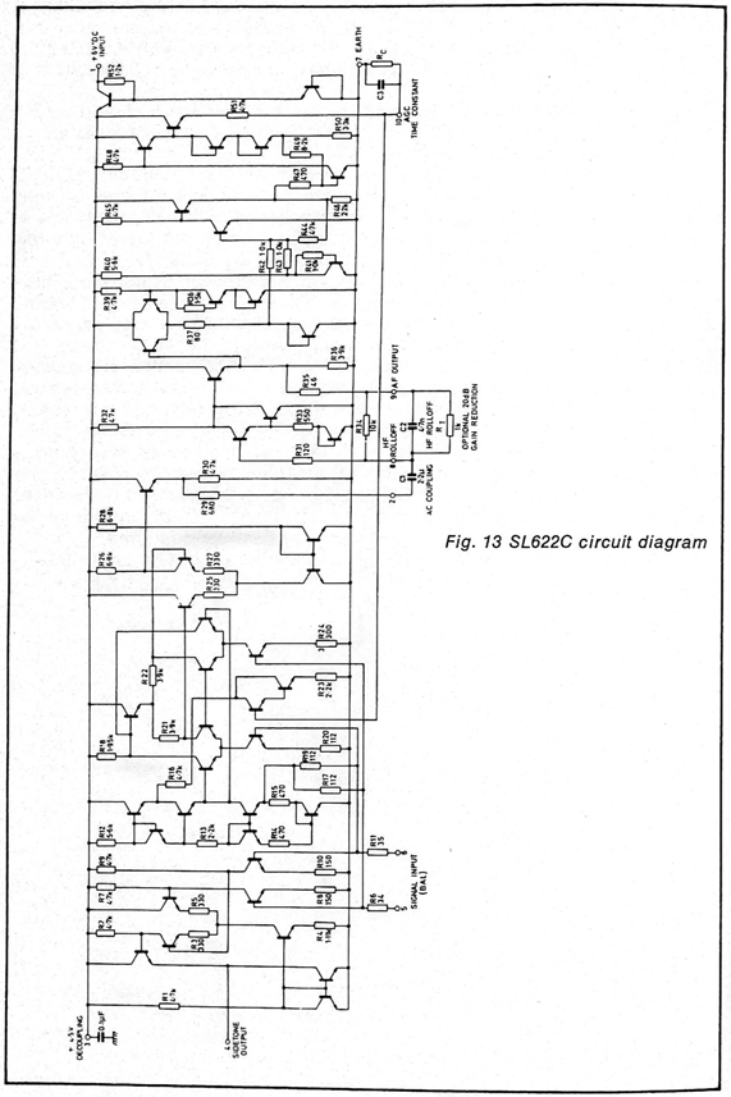


Fig. 13 SL622C circuit diagram

AF amplifier, VOGAD and sidetone amplifier

The SL622 and SL1626 are audio amplifier circuits with internal AGC designed to provide a constant output of about 100mV rms for 60dB of input range. In addition the SL622 has a separate sidetone output, not available in the SL1626.

When operated with single-ended input the SL622 and SL1626 have a dynamic range limited to about 40dB.

In general the following application notes apply to both these devices but there are some differences which have been noted.

Applications exist for these circuits wherever microphones are used: transmitters, intercommunication systems and telephone systems are obvious examples. They can also be usefully employed in radio receivers (in addition to the normal receiver AGC) to stabilise audio output.

CIRCUIT DESCRIPTION

The circuit consists of a two-section amplifier, AGC system, sidetone amplifier and voltage regulator. The SL1626 uses different circuit techniques to operate over the same supply range (+6V to +12V) without the use of a voltage regulator. Pin connections of the SL622 differ from those of the SL1626 which are shown in brackets.

CIRCUIT APPLICATIONS

Main Amplifier

The input stage is balanced and connected to pins 5(4) and 6(5). The input impedance is quite low (300 ohms balanced, 180 ohms single ended) and the inputs are self-biased. The pins may be connected together via a DC path or not, whichever is convenient, but they should not be connected to any other point at DC.

The dynamic range of the SL622 and SL1626 is about 40dB when driven single ended with the other input decoupled to ground. When driven push-pull with a balanced input, the range is about 60dB (100 microvolts to 100 millivolts rms).

AGC is applied just after the input stage and the output from the controlled stage coupled via a capacitor to the output stage. This capacitor sets the LF rolloff of the system.

A 2.2 microfarad capacitor, giving a 3dB point about 100Hz, is generally used. It is connected between pin 2(2) and 7(8); if a polarised capacitor is used the positive connection should be to pin 2. The HF rolloff is set by a capacitor between the output pin 8(9) and pin 7(8).

If the dynamic range of the circuit is too large (for instance in a mobile transmitter where vehicle background noise can be a problem) it may be reduced by placing a resistor between these two pins. The internal resistance between them is 10 kilohms and an external resistor of 1kilohms reduces the dynamic range to 40dB, 500 ohms to 34dB. The resistor should not be less than 500 ohms. The value of the HF rolloff capacitor depends on the value of

resistance between pins 7(8) and 8(9) and the 3dB frequency is the frequency at which the capacitive reactance equals the resistance. Hence, with no external resistor, a capacitor of 5nF is necessary for a 3dB point of 3kHz.

The output stage is an emitter follower and should therefore not be expected to drive a capacitive load. Its output impedance is about 50 ohms.

The AGC detector is connected to the main output and controls it to about 100mV rms. The AGC time constant is set by a resistor and capacitor in parallel from pin 1(10) to ground. The attack time constant is proportional to the capacitor, which should not be less than 22 microfarads, and is 0.4ms/microfarad. The decay time constant is proportional to the time constant of the resistor and capacitor and is 20dB/sec for a time constant of 50 seconds.The resistor should lie between 500 kilohms and 1.5 megohms. The usual values of R and C are 1 megohm and 50 microfarads which give about 20ms attack and 20dB/sec decay.

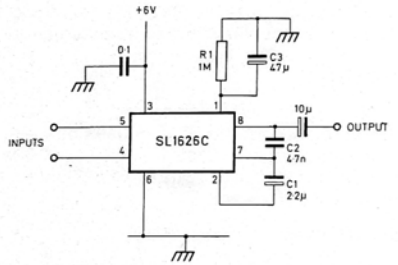


Fig. 14 Connection diagram for SL1626C used as a microphone amplifier

The problems associated with amplitude distortion inherent in simple VOGAD circuits have been largely overcome in the design of the SL622C. In certain circumstances, however, some distortion of the leading edge of the first spoken syllable can occur, but only after a considerable pause in speech. The effect is due to overshoot, which in turn results from capacitor C2 being allowed to discharge below the AGC threshold. In most applications however, the distortion is not of sufficient significance to justify the additional circuitry necessary for its elimination.

Since the device has only one earth connection for both input and output, care must be taken to avoid high impedance earth connections which might cause instability. In conditions where high RF fields may be encountered the can should be separately earthed to pin 7 or to a ground plane.

External Gain Control

Since the gain control voltage range of the SL622C is very small it is not really practicable to use the device as a VCA by applying a control voltage to the timing pin. However, the device can be easily muted by connecting the timing pin to +2V or held at full gain by earthing it. Some provision must be made for discharging C3 when the muting voltage is removed or the muting period will be prolonged until the capacitor has discharged through R1 (Fig. 14).

The Voltage Regulator (SL622C only)

The power supply is connected to pin 1; pin 3, which may be decoupled at LF to reduce supply ripple and improve sidetone linearity, is the +4.7V stabilised supply. It is recommended that pin 3 also be decoupled at HF by a 0.05 microfarad capacitor. Some users of the SL622C may wish to take small currents from pin 3 to other circuits requiring a stabilised supply. Whilst this is unlikely to harm the circuit if only one or two milliamperes are taken, the device may not perform to full specification. The current consumption of the integrated circuit rises from 14mA at 6V to 24mA at 12V.

Sidetone Amplifier (SL622C only)

The sidetone output is taken from pin 4 and is not frequency-shaped. The output impedance is 200 ohms and, like the main output, the sidetone output should not be used to drive capacitive loads.

SL623C, SL1623C & SL1625C

AM detector, AGC amplifier and SSB demodulators

The SL623C consists of an AM detector, an SSB detector and an AGC generator designed for use with AM. The SL623C was introduced to enable the small-signal sections of an HF AM/SSB transceiver to be completely integrated — all functions with the exception of the power amplifier can be realised with SL600 series integrated circuits. The outputs of the SL623C will drive most audio output stages with input impedances over 10 kilohms, and are particularly suitable for driving either the SL630C or the SL414A.

In addition to its audio outputs, the SL623C AGC generator is designed to control SL610/11/12 RF/IF amplifier strips, but, unlike the SL621C AGC generator, which operates from an audio signal, the SL623C control voltage is carrier-derived. It is therefore less suitable for use with SSB or CW. However, the AGC output pins of an SL621C and an SL623C may be connected together for an SSB/AM receiver, the gain then being controlled by the device with the higher output voltage.

The SL1625C is an SL1623C without its SSB detector.

CIRCUIT DESCRIPTION (Fig. 15)

The IF input is applied directly to one input of a full-wave detector and, via a unity-gain inverting amplifier, to the other input of the full-wave detector and to the signal input of a balanced demodulator. Two outputs from the full-wave detector are brought out of the package: audio and AGC. The AGC signal is used as the input to the AGC amplifier of the device. The AGC amplifier consists of two amplifiers in series. The first has a gain which may be varied between —0.25 and —5 by an external resistor and the second has a fixed gain of —20 and a frequency compensation point. The SSB detector, which requires a carrier input of 100mV rms, consists of a simple balanced de-modulator.

A single positive supply of between +6V and +9V is required. The supply should be decoupled close to the can by a 0.1 microfarad capacitor. Current consumption is approximately 10mA at 6V supply and zero AGC voltage, but rises with both supply voltage and AGC output level.

CIRCUIT APPLICATIONS

AM Detector

The detected AM output has an output impedance of about 1 kilohm and should be decoupled at RF with a 0.01 microfarad capacitor (C1). It should be connected to the audio stage via a dc blocking capacitor. The other detector output is similar but should be decoupled with a 50 microfarad capacitor (C2) to remove AF, and connected via a preset potentiometer R28 to the AGC amplifier input to provide rectified carrier for amplification as AGC. C1 and C2 should be connected directly to the earth pin via the shortest possible leads, which should not be common to any other components. C2 should have an AF series resistance of under 1 ohm and, if it does not also have a low RF impedance, should be shunted by a 0.01 microfarad RF bypass capacitor (C3). These measures prevent instability due to possible RF current loops.

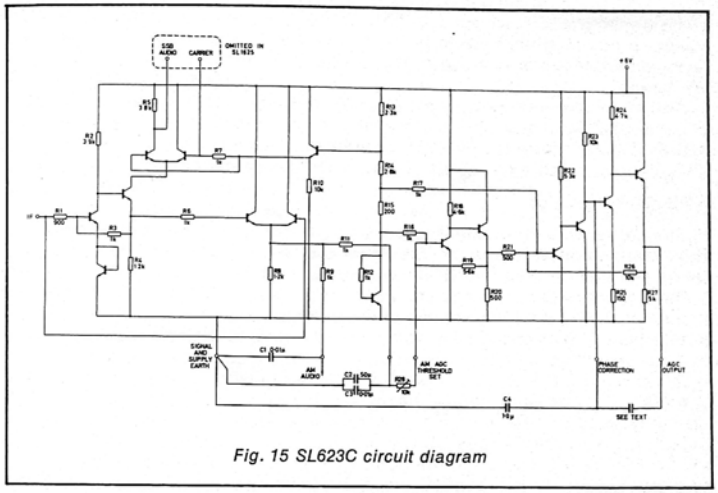


Fig. 15 SL623C circuit diagram

AGC Generator

Pin 3, the AGC amplifier phase correction point, should be decoupled to ground by a 1 microfarad capacitor (C4) ,keeping leads as short as possible. The value of C4 is quite critical, and should not be altered: if it is increased the increased phase shift in the AGC loop may cause the receiver to become unstable at LF and if it is reduced the modulation level of the incoming signal will be reduced by fast-acting AGC.

A capacitor connected to the phase correction point and the output of the AGC amplifier helps to reduce the ripple on the AGC output. Its value varies from system to system and with intermediate varying frequencies. Normally-used values vary between 0.1 and 10 microfarads. As there is no easy way to predict suitable values for particular systems, this component must be 'selected on test'.

The AGC output (pin 4) will drive at least two SL610/11/12 amplifiers and the 'S' meter circuit shown in Fig. 11. The SL623 AGC output is an emitter follower similar to that of the SL621C. Hence the outputs of the two devices may be connected in parallel when constructing AM/SSB systems.

Less signal is needed to drive the SSB demodulator than the AM detector. In a combined AM/SSB system, therefore, the signal will automatically produce an SSB AGC voltage via the SL621C as long as a carrier (BFO) is present at the input to the SSB demodulator of the SL623C. The AGC generator of the SL623C will not contribute in such a configuration.

For AM operation the BFO must be disconnected from the carrier input of the SSB demodulator. In the absence of an input signal, the SL621C will then return to its quiescent state. To switch over a receiver using the SL623C from SSB to AM operation it is therefore necessary to turn off the BFO and transfer the audio pick-off from the SSB to the AM detector.

Neglecting to disconnect the SSB carrier input during AM operation can result in heterodyning due to pick-up of carrier on the input signal. In some sets, different filters are used for AM and SSB; these will also need to be switched.

The 10 kilohm gain-setting preset potentiometer R28 is adjusted so that a DC output of 2 volts is achieved for an input of 125mV rms. There will then be full AGC output from the SL62C3 for a 4dB increase in input. A fixed resistor of 1.5 kilohms can often be used instead of the potentiometer.

SSB Demodulator

The carrier input is applied to pin 6, via a low-leakage capacitor. It should have an amplitude of about 100mV rms and low second harmonic content to avoid disturbing the DC level at the detector output.

Pin 8 is the SSB output and should be decoupled at RF by a 0.01 microfarad capacitor. The output impedance of the detector is 3 kilohm and the terminal is at a potential of about +2V which may be used to bias an emitter follower if a lower output impedance is required. The input to the audio stage of a receiver using an SL623C should be switched between the AM and the SSB outputs — no attempt should be made to mix them. Since the SL621C is normally used in circumstances where low-level audio is obtained from the detector, the relatively high SSB audio output of the SL623C must be attenuated before being applied to the SL621C. This is most easily done by connecting the SL623C to the SL621C via a 2 kilohm resistor in series with a 0.5 microfarad capacitor.

Input Conditions

The input impedance is about 800 ohms in parallel with 5pF. Connection must be made to the input via a capacitor to preserve the DC bias. An input of about 125mV rms is required for satisfactory carrier AGC performance and 20mV rms for SSB detection. Normally, the AGC will cope with this variation but in an extreme case a receiver using an SL623C and having the same gain to the detector in both AM and SSB modes will be some 10dB less sensitive to AM.

SL624C

Multimode detector

The SL624C was introduced to meet the very heavy demand for a single integrated circuit capable of demodulating all the common types of radio telephony — SSB, AM and FM. The SL624C amply satisfies these requirements and also contains an audio amplifier with voltage-variable gain capable of driving a simple output stage of several watts. Although it detects the modulation of the modes mentioned above the SL624C does not incorporate an AGC output, so it is normally used in conjunction with an SL621 and an SL613C to give AGC both on audio for SSB reception and on the carrier for AM and FM.

CIRCUIT DESCRIPTION (Fig. 16)

The SL624C multimode detector consists of a double-balanced modulator and a five-stage balanced limiting amplifier. There is also an audio amplifier, with voltage-variable gain, connected directly to the double balanced modulator output, and a separate audio amplifier with a voltage gain of 4 and a medium power output intended as an audio driver. The circuit requires a single positive supply of between +9V and +12V, which must be capacitively decoupled at RF. Current consumption varies with audio gain and also with the value of the output resistor on pin 15 but is in the region of 20mA at 12V. The circuit is usable at frequencies up to 30MHz.

The circuit functions as a quadrature detector of FM with the output of the limiting amplifier (which is driven by the receiver IF strip) applied via an LC phase shift network to the external input of the double-balanced modulator. Since the output of a double-balanced modulator is proportional to the phase difference between the inputs, the system acts as an FM detector. For good limiting a signal of about 200 microvolts is required at the limiting amplifier input.

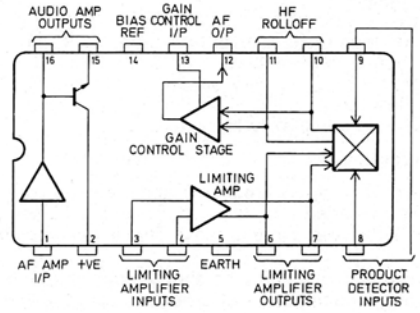


Fig. 16 Circuit diagram of SL624C

For AM the circuit acts as a synchronous detector. The output of the IF amplifier is applied to the limiting amplifier and to the modulator signal inputs. Since the carrier is separated from the modulation in the limiting amplifier, both carrier and signal are applied to the modulator, which therefore demodulates the signal. The input to the limiting amplifier should be greater than 2mV rms, with not more than 97 per cent modulation, to ensure that limiting occurs even on modulation troughs. A similar detector is used for SSB; the signal is applied to the external modulator input and the limiting amplifier is used as a BFO.

Considerable switching is necessary to switch between modes, particularly between FM and AM/SSB. Since the SL624C is not particularly expensive it is better to use two SL624Cs in a multimode receiver: one for FM, the other for AM/SSB. Whilst not absolutely necessary, this method is certainly less expensive in components and simpler in layout than using one IC for all three modes.

CIRCUIT APPLICATIONS

In view of the different systems in which the SL624C may be used this section is divided into two parts — circuit connection details and system details.

CIRCUIT CONNECTIONS

The positive supply is connected to pin 2 and pin 5 is earth. The supply must be decoupled within 2mm of pins 2 and 5 by a good quality, short-lead 0.1 microfarad capacitor. The supply voltage can be between 9 and 15 volts although at voltages above 12V dissipation can cause problems at high ambient temperatures.

Audio Amplifier

This amplifier has a voltage gain of 12dB (4 times) between the input on pin 1 and the outputs on pins 15 and 16. The input resistance at pin 1 is about 50 kilohms and signals should be applied through a capacitor. The output impedance at pin 16 is 4 kilohms and the DC potential is approximately half the supply voltage.

Pin 15 is the free emitter of an emitter follower with its base connected to pin 16. An external load resistor must be connected if the emitter follower is to be used. The output impedance at pin 15 can be as low as a few tens of ohms so the output can drive very simple output stages directly. Such an output stage is illustrated in Fig. 17a. For output stages running on lower voltages slightly more complexity is necessary.

Limiting Amplifier

The limiting amplifier inputs are pins 3 and 4 and its outputs pins 6 and 7. It consists of five cascaded long-tailed pairs and is biased by DC feedback from pin 7 to pin 4 and from pin 6 to pin 3. This is accomplished as shown in the Fig. 17b.

All the leads involved should be as short as possible and C1 and C2 must be earthed as close to each other and to pin 5 as possible to prevent instability due to RF earth currents. R1 can be any convenient value from 10 ohms to 10 kilohms and serves to prevent the input to the amplifier being earthed by

C2. The input can also be applied to pin 4 if this is more convenient in which case R1 would be placed between C1 and pin 4. If a balanced input is required two resistors are necessary.

The limiting amplifier can handle signals up to 30MHz and limits with inputs of over 100 microvolts rms. As the gain varies with temperature, signals of about 300 microvolts rms are required to ensure limiting at temperatures from —55°C to +125°C.

The open loop gain of the amplifier is about 70dB. When considered with its 30MHz bandwidth it is evident that great care must be taken to separate the input and output circuits to prevent instability. Another measure to prevent instability is to ensure that pins 6 and 7 are not loaded with less than 2 kilohms of resistance or more than a few picofarads of capacitance.

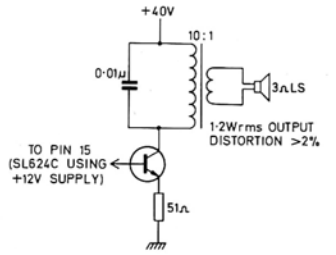


Fig. 17(a) Simple output stage

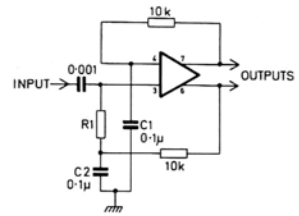


Fig. 17(b) Limiting amplifier bias arrangement

Double Balanced Modulator

This part of the circuit is essentially similar to the SL640C. The limiting amplifier outputs drive the carrier inputs of the modulator and are also brought out on pins 6 and 7 but it must be noted that these terminals must not be used for injecting a carrier signal from an external source. The signal inputs, connected to pins 8 and 9, have an input impedance of 2 kilohms plus 3pF each and are internally biased. It is quite permissible to have a DC path between pins 8 and 9 but it is not necessary; there should be no DC path from either pin to any other point, however. Signal inputs to the modulator may be balanced or unbalanced; in the first case the signal is applied to pins 8 and 9 in antiphase, in the second one of the pins is decoupled to earth by 0.1 microfarad while the other has the signal applied to it.

As explained in the SL640 circuit data the output of a double-balanced modulator with two signals at frequencies f_1 and f_2 applied to it consists of two frequencies: $|f_1+f_2|$ and $|f_1 - f_2|$. In the normal use of the SL624C, $|f_1+f_2|$ will be several MHz and $|f_1 - f_2|$ will be an audio signal. The earlier the RF signal is eliminated the less likely it is to produce undesirable effects; a capacitor of 0.01 microfarad or so connected within 2mm of pins 10 and 11 should be sufficient. This capacitor also produces 6dB/octave audio roll-off above 3kHz.

Audio Gain Control Stage

The audio gain control circuit is internally connnected to the modulator.A the voltage on pin 13 increases from a reference voltage (pin 14) to 12V the gain of this stage increases by 80dB. The resistance at pin 13 is 5 kilohms and the output impedance of the stage (pin 12) is 3 kilohms. This stage may be used in either or both of two modes: as a muting stage or as a volume control. When used only as a mute, pin 13 is connected to earth when the audio is to be muted, otherwise to +12V. This may be done electronically by a squelch system or by a switch.

The volume control system uses a 47 kilohm log potentiometer between pins 2 and 14 with the wiper connected to pin 13, a system which gives an approximately logarithmic gain control law. To achieve both volume control and mute the positive side of the potentiometer must not go directly to pin 2 but to the positive supply via the mute switch, (whether electronic or manual).

DETECTOR SYSTEMS

Four systems are described: FM, AM, SSB and AM/SSB switched. A squelch circuit useful for AM and FM reception and AGC systems usable with all three modes will also be described.

FM Detector

An FM detector is shown in Fig. 18. Basically, the signal is fed to the limiting amplifier and then, via a frequency-sensitive phase shift network, to the modulator. Since the output of the modulator is proportional to the relative phase of its two inputs, and since the phase of the external input, having passed the phase shift network, is proportional to frequency, the system acts as an FM detector.

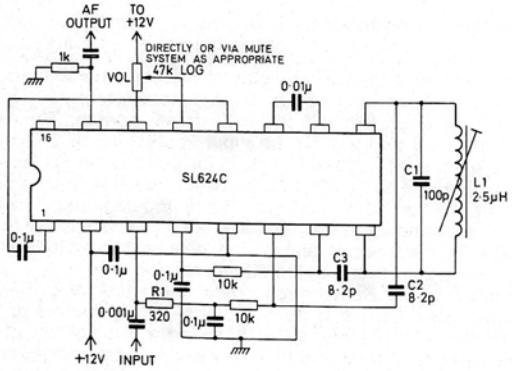


Fig. 18 FM detector

The system illustrated operates at 10.7MHz; to operate at other frequencies, L, C1, C2 and C3 must be scaled accordingly. The circuit can be used at frequencies from 445kHz to 30MHz, but it may be necessary to introduce a resistor between pins 8 and 9 to reduce the Q of the phase shift network if $\Delta f/f$ (the percentage deviation) becomes too great. The detector may thus be used for commercial FM broadcast reception or for television sound sub-carrier demodulation.

The SL624C was developed from television circuits and the impedance loading the Q of the quadrature coil is quite low. If a high Q quadrature circuit is necessary (as it is for narrow deviations at high IFs) the SL624C should be replaced with the SL664C or the SL665C.

An input of at least 100 microvolts rms is required, but 200 microvolts rms or above is preferable. If an impedance match is required for any reason, R1 may be any value between 10 ohms and 10 kilohms.

The only adjustment required is the tuning of the phase-shift circuit. An FM signal of the correct centre frequency and with as large a deviation as the system is expected to handle is applied and the tuned circuit adjusted to obtain an undistorted audio output. There are three possible settings of this adjustment since the phase-shift characteristic has an S-Curve. The centre one of the three should be used since, although it may give a lower output than the other two, it will be least distorted and best able to survive long-term ageing of components.

The output will be high level noise if the limiting amplifier has insufficient input and does not limit. To prevent this condition, the squelch circuit shown in Fig. 19 is used. This circuit detects the limiting amplifier output and, if modulation is present (indicating that the amplifier is not limiting), mutes the detector audio stage. The squelch can be used with both the FM and AM detectors but not with the SSB detector.

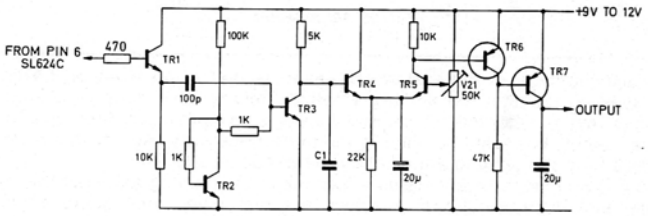


Fig. 19 Squelch system. Note: TR1 to TR5 is a Plessey SL3045 5-transistor array (discrete transistors are not suitable), TR6 and TR7 are discrete PNP types. C1 should be between 100pF and 5000pF, depending on permissible system noise; VR1 sets the squelch level.

AM Detector

The AM Detector illustrated in Fig. 20 is a synchronous detector, i.e. the carrier is separated from the modulation by the limiting amplifier and is then mixed with the whole signal in the modulator to give a demodulated audio output. Such a system has a great advantage in modern receivers (where a single block filter precedes a high gain broadband IF amplifier) in that nearly all noise products (produced by the modulator mixing the incoming carrier with broadband noise from the IF amplifier) are out of the audio range and are therefore, not available. With an envelope detector — such as a diode — all this noise is detected, much of it within the audio passband, and the detector performance is degraded.

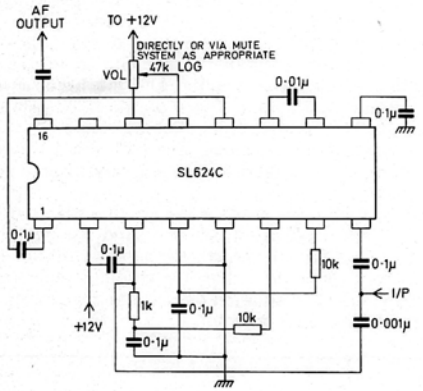


Fig. 20 AM detector

A disadvantage of the system, however, is that if the level of the input signal is so low that the limiting amplifier fails to limit during modulation troughs severe distortion occurs, and if there is no input signal there is a large noise output. Adequate squelch is therefore necessary. Again, this may be derived from the limiting amplifier by the circuit Fig. 19.

To ensure that sufficient signal is applied to the limiting amplifier the input signal amplitude should be at least 2mV rms. Even then some difficulty may be experienced with signals having over 97 per cent modulation — but such signals are not usual. An input signal of 5mV is a good target value but the detector will handle signals up to 50mV without difficulty. To keep the input within this range AGC is required. In a speech system an audio AGC such as the SL621C (its sensitivity modified by a series input resistance) is ideal. Its only drawback is that if an unmodulated carrier is received no AGC is produced and the amplifiers in the system can overload. Therefore the better system to use is that shown in Fig. 21. In this circuit an SL621 normally controls the system to hold the audio output constant, and if an unmodulated

carrier is received the extra RF detector provides sufficient AGC to prevent the IF amplifier from saturating. A big advantage of this system over the simple carrier AGC used in most AM receivers is that the audio output does not vary with modulation depth — thus, the volume control need rarely be adjusted.

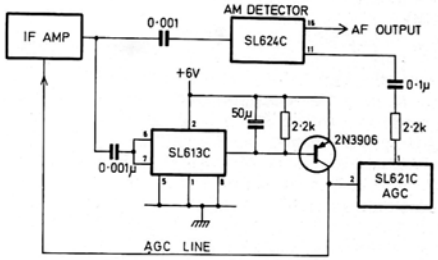


Fig. 21 AGC system

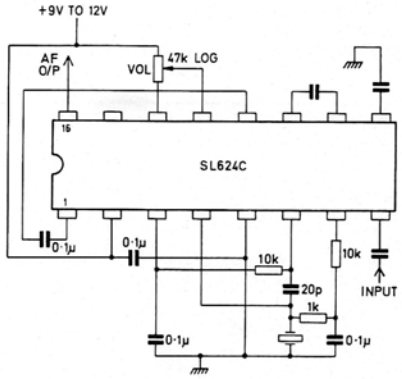


Fig. 22 SSB detector — self-oscillating

SSB Detector

In the SSB detector of Fig. 22 the limiting amplifier is connected as a BFO and the signal input is applied to the modulator input. The system is similar to the AM system above except that the carrier is generated by an oscillator rather than recovered from the signal. The input signal requirement is again 50mV maximum but in this case inputs lower than 5mV can be tolerated if the resulting lower output is acceptable. Carrier squelch is not possible — if squelch is required it must be derived from the SL621C AGC system, but since the BFO runs continuously detected noise is less of a problem and squelch is not really necessary.

AM/SSB Detector

This detector consists of an AM detector as described above, with a separate input on pin 4. During AM reception this input is not driven, but during SSB reception it is driven with a 200mV signal from a separate BFO. This swamps the input on pin 3 and the device acts as a product detector.

It is possible to make the internal limiting amplifier function as a switched limiting amplifier/BFO but this presents layout difficulties. It is much easier to use an extra transistor as a BFO.

SL630C & SL1630C

Microphone/headphone amplifier

The SL630C is an audio amplifier having 40dB gain and an internal gain control of approximately 60dB, and an output capability of 200mW into a 40 ohm load when used with a 12V supply. The SL630C is designed for use with the SL620C AGC generator.

CIRCUIT DESCRIPTION AND APPLICATIONS

To maintain HF stability — particularly on negative half-cycles — the output (pin 1) should be decoupled by a 1,000pF, low series inductance, capacitor placed directly between pins 1 and 10 (8) with leads cut as short as possible. This component must be on the integrated circuit side of the output coupling capacitor. At high supply voltages and/or low temperatures 10 ohms must be placed in series with this capacitor and 100pF connected from pin 4 to earth. The output is coupled to its load with a capacitor of a low impedance relative to the load at the lowest frequency to be used. The load may be resistive or reactive and, for maximum power output, should lie on the load/supply voltage line. *Any higher value of load impedance is quite safe but the device will over-dissipate and eventually destroy itself by overheating if the output is short-circuited.* The optimum load therefore, at any rate with supplies of over 9V, can be regarded as a safe minimum. The circuit shown in Fig. 23 which shows the SL630C used as a headphone amplifier, may also be used with loudspeakers having suitable impedances. The distortion is about 0.5 per cent at full output.

The power supply, to pin 2, should be between +6V and +12V and adequately decoupled both at HF and LF. The quiescent power consumption at various supply voltages is shown in the Power characteristics, as is the relation of the supply voltage to the optimum load and the maximum power available.

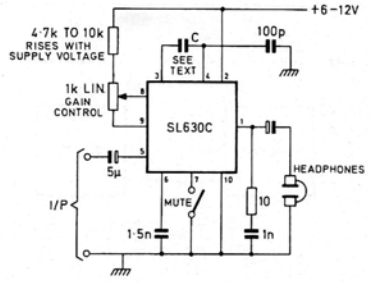


Fig. 23 Headphone amplifier using the SL630C

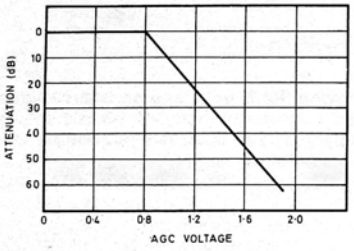


Fig. 24 AGC characteristics

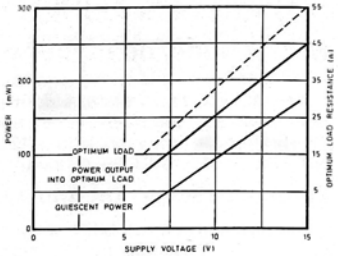


Fig. 25 Power characteristics

A capacitor connected to pins 3 and 4 defines the high frequency response of the amplifier. The upper 3dB frequency, f, is given by the formula:

$$f = \frac{16000}{C+20} \text{ kHz. (C is in picofarads)}$$

Pins 5 and 6 are input terminals. They may be used together as a differential input, in which mode they present an impedance of approximately 2 kilohms and result in a voltage gain (without gain control) of 100 (40dB). When the input is obtained from a magnetic transducer or a transformer it is desirable to use the differential input mode since the signal winding may be connected directly between pins 5 and 6 and no other components are required. This input is also recommended when the SL630C is being used with an SL620C in the automatic gain control system described below (Fig. 26), but in this case it is best to connect 0.25 microfarads in series with the signal winding to minimise offset effects when AGC is applied. *Pin 6 should always be decoupled at RF by 1500pF to earth.*

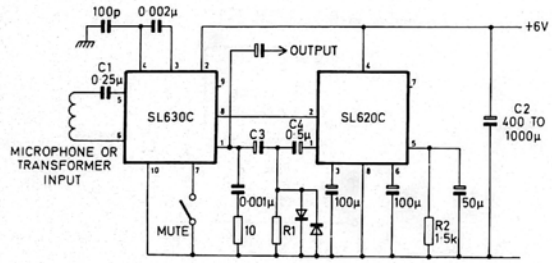


Fig. 26 Audio amplifier with AGC

An input may also be applied between pin 5 and earth. In this case the gain is 200 (46dB) and the input impedance 1 kilohm. Pin 6 should be earthed by 1500pF. A coupling capacitor is required between the input and pin 5.

The circuit is muted by earthing pin 7. A muted circuit attenuates an input by about 100dB. There is no mute facility on the SL1630.

Gain control is applied to pin 8, (7) which has an input impedance of 3.6 kilohms. It must be appreciated that even with full gain control the input cannot exceed 50mV rms without clipping so that at high control levels the output level is limited. The AGC characteristics will vary with temperature but, as shown in Fig. 23 a potentiometer to give manual gain control can be connected to the internal bias point at pin 9 which provides a temperature-compensated reference at the voltage at which gain control commences. This reference pin is omitted on the SL1630C. Pin 10 (8) is the signal earth and negative power supply connection.

The SL630C used with an SL620C in an AGC controlled circuit is shown in Fig. 26. With regard to this application, the following points should be noted:

1 The time constant R1C3 must be 800 microseconds and R1 must not exceed 300 ohms. Within these limits R1 may be the external load but if the external load impedance is likely to vary or be larger than 300 ohms it should be connected directly to pin 1 via an appropriate capacitor and R1 and C3 should be separate.

2 C1, whose use is not essential, reduces the risk of motor-boating (VLF oscillation). If an electrolytic capacitor is used it may be connected with either polarity as there is only 10mV across it.

3 R2 is also non-essential but is useful if the input is likely to contain a large component below 300Hz.

4 C2 should be used if the power supply has a source impedance of more than a few ohms or is connected by long leads.

SL640C, SL641C, SL1640C & SL1641C

Double balanced modulators

A Modulator is a device the output of which is the product of its two inputs. Modulators are extensively used as frequency changers, phase detectors and in many other applications. If two frequencies, f_1 and f_2, are applied to the inputs the output consists of the frequencies $|f_1 + f_2|$ and $|f_1 - f_2|$.

Many types of modulator are known, rather fewer are in common use. The most common is probably the diode ring – this has the advantages of good signal and carrier rejection and simple structure. It also has several drawbacks: it must be set up carefully, it needs two or three tuned transformers, its gain is less than unity and it needs a high level signal to one of its inputs.

The transistor double-balanced modulator, of which the Plessey SL640C and SL641C are examples, is less well-known than the diode ring, despite several advantages. This is because, until the advent of integrated circuits, it was too complex and expensive a procedure to accomplish the matching necessary to make a double-balanced modulator with transistors. Transistors in integrated circuits, however, are intrinsically well-matched so that, if a double-balanced modulator is made as an integrated circuit, little if any external balancing is necessary. Furthermore, and in contrast to a diode ring, such a modulator needs little setting up, no transformers or tuned components, and only low-level inputs. Its gain may be greater than unity.

PRINCIPLES OF OPERATION

A simple double-balanced modulator is shown in Fig. 27. It is evident that the sum of the two output currents equals the tail current and that, from considerations of symmetry, if either V1=V2 or V3=V4 then I1=I2. Also if R is much greater than R_e the collector currents of TR1 and TR2 will differ by an amount proportional to the difference between V1 and V2. If, therefore, a small input at frequency f_1 is applied between V1 and V2 and a large signal at f_2 is applied between V3 and V4, sufficient to turn the transistors TR3, TR3, and TR4, and TR4, fully on and off, it is evident that switching modulation, similar to that of a diode ring will occur and frequencies $|f_1 \pm f_2|$ will occur at the output as will sums and differences of f_1 and the odd harmonics of f_2 i.e. $|f_1 \pm 3f_2|$, $|f_1 \pm 5f_2|$, etc.

CIRCUIT DESCRIPTION AND APPLICATIONS

The circuits of the SL640C and SL641C are very similar but have different signal input and output configurations — these are fully discussed below.

The circuits require a single, well-decoupled positive supply of between 6 and 9 volts and consume about 12mA. Pin 2, an internal bias point, must also be decoupled by a low-leakage (less than 100nA) capacitor having a low reactance at the lowest signal or carrier input frequency.

Pin 1, which is connected to the can, should be earthed to prevent HF pickup.

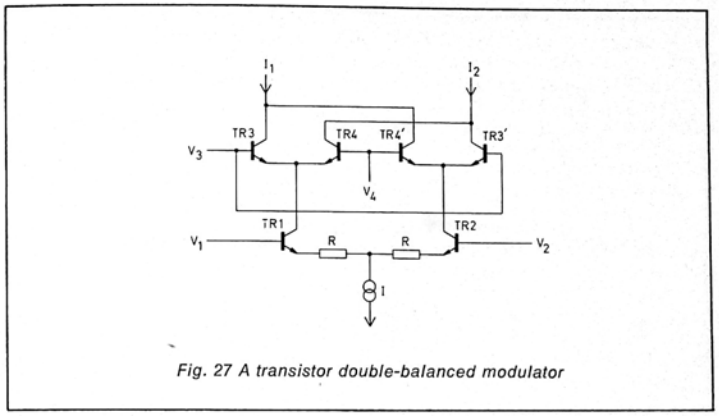


Fig. 27 A transistor double-balanced modulator

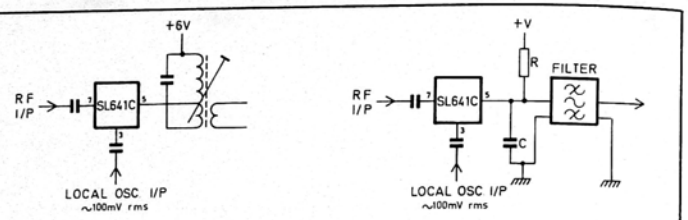
The input and carrier signals, which should not exceed 200mV rms, are applied to pins 7 and 3 respectively. Both the SL640C and the SL641C have a carrier input impedance of 1 kilohm and 4pF and the SL641C has a similar signal input impedance. The signal input impedance of the SL640C is 500 ohms and 5pF. The input coupling capacitors should have a leakage of less than 100nA and an impedance of less than 100 ohms at the lowest frequency they will carry. This should be reduced to less than 10 ohms above 10MHz.

The output of the SL641C is intended as a current drive to a tuned circuit. If both sidebands are developed across this load its dynamic impedance must be less than 800 ohms. If only one sideband is significant this may be raised to 1600 ohms and it may be further raised if the maximum input swing of 200mV rms is not used. The DC resistance of the load should not exceed 800 ohms. If the circuit is connected to a +6V supply and the load impedance to +9V, the load may be increased to 1.8 kilohms at AC or DC. This, of course, increases the gain of the circuit.

There are two outputs from the SL640C; one is a voltage source of output impedance 350 ohms and 8pF and the other is the emitter of an emitter follower connected to the first output, which requires a discrete load resistor of not less than 560 ohms. The emitter follower output should not be used to drive capacitive loads as emitter followers act as detectors under such circumstances with resultant distortion and harmonic generation. Frequency-shaping components may be connected to the voltage output and the shaped signal taken from the emitter follower.

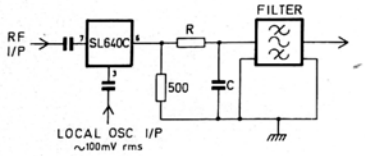
The circuits will operate with input frequencies between 1Hz and 70MHz with the specified performance; the SL641C will operate at up to about 150MHz with reduced performance. To use them at frequencies below 100Hz precautions must be taken to prevent leakage in the input coupling capacitor from altering the device bias.

Some applications of the SL640C and SL641C are shown in Figs. 28 and 29. Power, decoupling, and earth connections are not shown.



(a) *SL641C with LC IF filter*

(b) *SL641C with crystal filter*



(c) *SL640C with crystal filter*

Fig. 28 SL640/41C receiver mixer circuits

Fig. 28a shows the SL641C used as a receiver mixer driving a wound IF coil. Fig. 28b shows it driving a crystal filter. R and C must be selected to match the filter. If R is less than 800 ohms it may be connected to the +6V line supplying power to the SL641C; if it is between 800 ohms and 1.8 kilohms it should be connected to +9V (while the SL641C supply must remain at +6V). If R is greater than 1.8 kilohms the circuit in Fig 28b is unsuitable and the SL640C circuit illustrated in Fig. 28c should be used.

The SL640C and SL641C have a noise figure of about 10dB at 100 ohms source impedance. When used as receiver mixers they have better than —40dB intermodulation products so long as unwanted signals do not exceed 30mV rms. Thus, either can be used as a receiver mixer at HF without an RF amplifier since atmospheric noise will far exceed device noise at these frequencies if the antenna is reasonably good. If an SL610C RF amplifier is used the intermodulation threshold will be reduced to 3mV rms (since the SL610C has a gain of 10). The SL640/41 is then less attractive as a mixer and a diode ring mixer should be used.

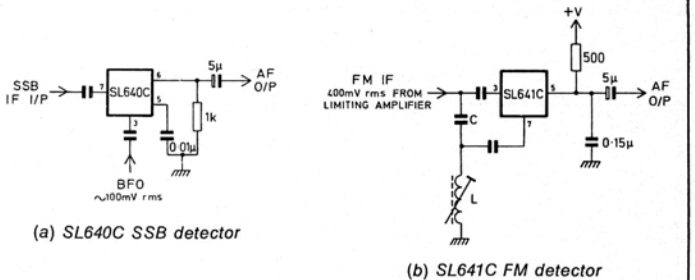
Fig. 29a shows the SL640C used as an SSB detector. The capacitor connected to output pin 5 decouples the sum frequency $|f_1 + f_2|$, while the audio difference frequency $|f_1 - f_2|$ is taken from pin 6. An FM detector is shown in Fig. 29b but the function is better performed by a Plessey Semiconductors SL665 integrated circuit, which has its own limiting amplifier. The phase comparator shown in Fig. 29c is more useful — it may be used as a detector for phase modulated signals or as a comparator in phase-locking systems such as frequency synthesisers.

Signal and carrier leak may be reduced by altering the bias on the carrier and signal input pins, as shown in Fig. 29d. With carrier but no signal R1 is adjusted for minimum carrier leak. A similar network is connected to the carrier input and with signal and carrier present, signal leak is minimised by means of R2.

Fig. 30a shows the SL640C or SL641C used as a sideband generator. Both sidebands are produced so that if a single sideband is required it must be obtained by subsequent filtering (Fig. 30b). If pin 2 is earthed by a resistor of about 15 kilohms (its actual value may need to be selected) the device's carrier leak is increased to a point where the DSB signal becomes AM. This is useful where it is desired to select sideband or AM. In the circuit shown in Fig. 30c a single sideband only is produced. It is important that both the audio and carrier reference and quadrature signals should be accurately 90 degrees out of phase. The amplitude of one phase of audio should be adjusted to obtain maximum second sideband rejection.

If the carrier reference is connected to input A, and the carrier quadrature to input B, LSB output results. If the carrier quadrature is connected to input A, and reference to input B, USB output results.

Many other applications of the SL640C and the SL641C are possible, such as speech scramblers, and electronic music generators. The devices may, in fact, be used wherever multiplication, phase sensitive detection or frequency changing are required.



(a) *SL640C SSB detector*

(b) *SL641C FM detector*

(c) *SL640C phase comparator*

(d) *Signal and carrier leak adjustment*

Fig. 29 SL640/41C detector circuits

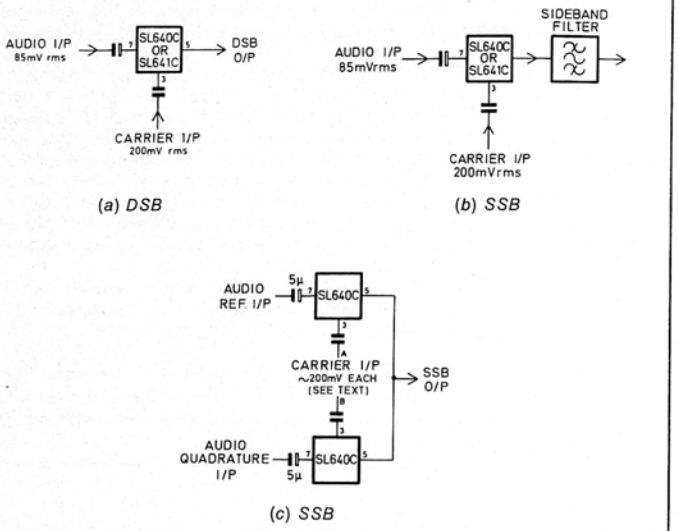


Fig. 30 Sideband generators

SL664C & SL665C

FM receiver IF and detector systems

The SL664C and SL665C each form the complete IF detector system for a narrow band FM receiver. They use little power and have a sensitivity of about 10 microvolts. In addition the SL664C has a 250mW output stage. Unlike most integrated circuit quadrature detectors they do not load their quadrature elements and a S/N ratio of over 50dB is possible with a 1.5kHz deviation at an IF of 10.7MHz.

CIRCUIT DESCRIPTION AND APPLICATIONS

The SL664C and the SL665C are illustrated in Fig. 31. Each consists of an IF preamplifier with a 25MHz bandwidth, a main limiting amplifier with similar bandwidth, a quadrature detector, a squelch system, and a DC audio gain control. In addition, the SL664 contains an audio output stage supplying 250mW to an 8 ohm loudspeaker.

The IF preamplifier has a bandwidth of 25MHz, a voltage gain of about 46dB and an input impedance of about 5 kilohms in parallel with 2pF. It consists of five cascaded long-tailed pairs and has excellent limiting characteristics.

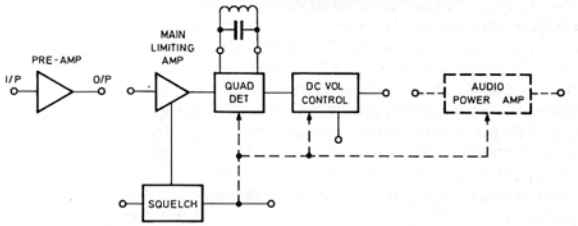


Fig. 31 Block diagram of SL664 & SL665. (Dashed detail applies to SL664 only)

The main IF amplifier also has a bandwidth of 25MHz but its voltage gain before limiting is about 60dB and it consists of six long-tailed pairs. Two of these stages (numbers 3 and 6) contain detectors, the output of which feed the squelch system. The output of this limiting amplifier feeds a double balanced modulator and also an external phase shift circuit which in turn feeds the other port of the double-balanced modulator. This double-balanced modulator thus acts as a quadrature detector. The quadrature detector has particularly good performance when demodulating narrow band FM signals with a high IF because the impedance of the quadrature ports is high (over 50 kilohms) and so the Q of the quadrature circuit is not impaired by being loaded, as is so often the case with integrated circuit quadrature detectors.

The audio output from the quadrature circuit goes to a DC controlled audio amplifier and so allows the use of remote gain control The output of the SL665C is taken from this gain control.

The squelch system is driven by the detectors in the IF strip and contains a comparator which requires an external squelch level program. A resistance between this program input and the squelch output provides hysteresis to the system. In the SL665C the squelch system only provides a DC output to indicate the presence of a signal larger than the squelch threshold but in the SL664C the squelch also turns both the detector and the audio stages on and off. This means that the SL664C has a lower standby power consumption despite being a more complex circuit.

The SL664C is manufactured in an 18-lead ceramic DIL package, the SL665C in a 16-lead ceramic DIL package. The two devices are designed so that they may be used on the same printed circuit board in different radios – i.e. pins 1 to 6 of both devices are identical and pins 13 to 18 of the SL664C are identical to pins 11 to 16 of the SL665C. Only the connections to the pins at the end of the package remote from the index slot differ between the two devices. In the pin by pin application notes which follow the pin numbers will be given for the SL664C and the pin numbers for the SL665C, if they differ, will be given in brackets.

Pin 1 is the bias point for the main IF amplifier. It must be decoupled effectively by an RF capacitor to ground and connected by a resistor or coil to the IF input pin 14(12). If a resistor is used it should provide the correct match for the interstage filter. If a coil is used it will be part of a filter and must not have any DC connection to ground.

The decoupling capacitor should be at least 0.01 microfarads and with lower IFs (such as 455kHz) should be 0.1 microfarads or more.

Pin 2 is the squelch programming point and pin 3 the squelch output pin. The squelch is programmed by a 470 kilohm variable resistor (which should be increased to 1 Megohm if supplies over 6V are used) in series with a 47 kilohm fixed resistor connected between pin 2 and earth. Squelch sensitivity increases with the value of the variable resistor. In the absence of a signal, pin 3 is at high potential which falls when a signal is present. The output capability of pin 3 is only 2mA but it may be buffered if necessary.

The decoupling capacitor of 0.33 microfarad prevents brief breaks in signal (such as a mobile 'flutter') from squelching the circuit. Hysteresis in the squelch is obtained by a resistor between pins 2 and 3. The amount of hysteresis depends on the squelch threshold, the resistor value, and the supply voltgage. At 6V supply a 360 kilohm resistor gives 2 to 3dB hysteresis at 10 microvolts squelch level and about 10dB at 100 microvolts. Larger resistors are necessary at higher supply voltages and the minimum possible hysteresis rises to about 7dB with a 1.5 Megohm hysteresis resistor and a 9V supply.

Despite its variation with supply voltage, the squelch is quite stable with temperature, and alters by only 1 to 2 dB as the circuit is temperature-cycled. If squelch is not required the SL665 squelch pins may be used, with an SL3046 transistor array, to drive an 'S' meter as shown in Fig. 32. The system consists of a negative feedback amplifier and is not possible with an SL664C, where the internal squelch must always be used.

The quadrature circuit is connected between pins 4 and 5. This can consist of an LC tuned circuit resonant at the centre of the IF passband, or one of the commercial quadrature elements for NBFM; even a ceramic interstage filter

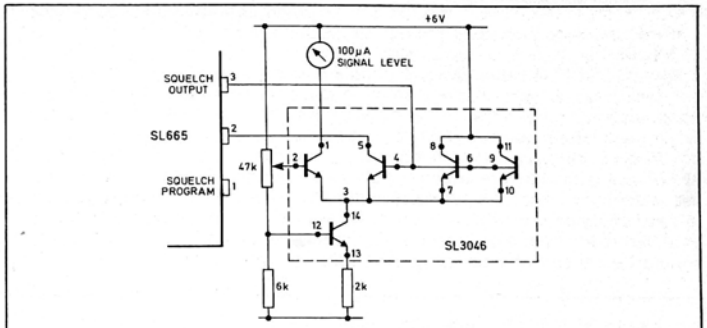


Fig. 32 "S" meter circuit for use with the SL665C

such as is made for broadcast applications can be used. Ceramic filters usually need to be tuned by a parallel trimmer capacitor; their efficiency as a quadrature element can vary widely from batch to batch so they are not, perhaps, the best elements to use although they are shockproof and smaller than a coil.

The resistive element of the impedance between pins 4 and 5 is over 50 kilohms and has little effect on the Q of the quadrature element. Narrow deviation FM can therefore be demodulated with excellent signal to noise ratio. Should a lower Q be required for wider FM a resistor may be connected in parallel with the tuned circuit.

There must not be a DC path between pins 4 and 5 and any other point, but they themselves may be connected together or not as is convenient. In the limit it is better to have a DC path between them than not, but this should not be at the expense of the Q of the quadrature element.

The DC volume control consists of a fixed resistor of 47 kilohms in series with a variable one of 470 kilohms connected between pin 6 and ground. The audio range is typically 70dB (3000:1) and gain is a minimum when the resistance is minimum.

Pins 7 to 11 of the SL664C and pins 7 to 10 of the SL665C are different and will be dealt with at the end of this section.

Pins 12 and 13 are the SL664C supply pins; pin 12 is the audio output stage supply pin while pin 13 supplies power to the rest of the circuit. In the SL665C, pin 11 is the only power supply connection.

The supply voltage is normally 6V but the circuit will work with supplies between 5 and 12 volts with little change in performance. Consumption at 6V is 3mA (squelched) and 10mA (unsquelched) for the SL664C and 6mA in either case for the SL665C. If the audio output stage of an SL664C is not required the power supply on pin 12 may be left unconnected.

The power supplies must be well decoupled at RF with at least 0.1 microfarad RF capacitors having short leads and should have low ripple at audio frequencies. The SL664C should be decoupled as near to the device as possible with a large electrolytic capacitor as well, otherwise AM rejection tends to suffer.

Pin 14(12) is the input of the main IF amplifier and should be connected to pin 1 as described above. The input impedance is about 5 kilohms in parallel with 2pF.

Pins 15 and 17 (13 and 15) are decoupling points within the circuit and should be decoupled to ground by good RF capacitors, preferably 0.1 microfarads. Insufficient decoupling at these pins causes poor AM rejection and in the worst case can cause instability or oscillation.

The bias circuitry for both the main amplifiers and the preamplifier is shown in Fig. 33. The preamplifier input is pin 16(14). It is not self-biased but is fed with bias from pin 18(16) via a total of 15k ohms. The input impedance of the preamplifier is 5 kilohms in parallel with 2pF. If, as is common, the preamplifier is fed from a filter requiring a precise match, the value of resistor R2 should be chosen appropriately. It should not exceed 800 ohms.

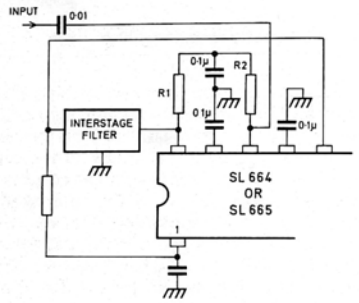


Fig. 33 Bias circuit for the SL664 and SL665C

The preamplifier output is pin 18(16) and has an output impedance of 300 ohms. Signal is taken from pin 18(16) to the input of the main IF amplifier via an interstage filter. This filter is to provide some limitation of noise bandwidth and need neither have a good shape factor nor a large stop-band attenuation. Any simple filter is suitable but at 10.7MHz cheap ceramic filters are particularly useful as they are small and require no setting up. Murata SFE 10.7MA filters are recommended here since they match the output impedance of the preamplifier.

The noise figure of the preamplifier is 7dB with a source impedance of 350 ohms. Signal is fed to pin 16(14) via a capacitor or other DC blocking component.

Pins unique to the SL664C

The final part of this section deals with those pins whose functions differ between the SL664 and SL665.

The SL664 pin 7 is the DC audio gain control output and is fed by an emitter follower with a low current tail. Hence (although it has quite a low output impedance) it cannot drive a very low impedance load. An HF rolloff capacitor

to ground is connected from this pin and should have a value of 0.3 microfarads/f where f is the desired rolloff frequency in kHz. In normal use pin 7 is connected to pin 8, the input to the output stage, by a 0.1 microfarad capacitor. Pin 8 is biased by connecting it to the centre of two 240 kilohm resistors connected in series between the positive supply and earth.

Pin 9 of the SL664C is the inverting input to the output stage and provides negative feedback to define the stage gain. The feedback resistor from the output should be 120 kilohms. The gain-defining resistor from pin 9 to earth via 22 microfarad capacitor is usually around 12 kilohms but may be increased to reduce gain or vice-versa. Pin 10 is earth and pin 11 is the audio power output. The output is decoupled to earth with 0.22 microfarads to ensure HF stability and drives its load via a 100 microfarad capacitor. The feedback resistor, in order to provide DC bias is connected directly to pin 11.

Pins unique to SL665C

Pin 7 of the SL665C is not used and neither is pin 9. Pin 8 is ground and pin 10 is the audio output. This output appears on the collector of a transistor so must be connected to the positive supply by a resistor – generally 10 kilohms. Audio is taken through a capacitor and the pin must also be decoupled at HF by a capacitor of 0.015 micrfarads/f where f is the cutoff frequency in kHz.

SL680C & SL1680C

Crystal oscillator maintaining circuits

The SL680C is a circuit designed to maintain oscillation in an external series resonant crystal without significant degradation of frequency stability. Its output is a sinewave with about 3 percent THD with level independent of crystal activity. The SL680C may be used in fundamental or overtone oscillators.

CIRCUIT DESCRIPTION

A block diagram of the SL680C is shown in Fig. 34. It consists of a common-emitter transistor amplifier with emitter decoupling provided by the quartz crystal. The output of this stage is coupled externally, by a capacitor or a tuned circuit (depending on whether fundamental or overtone operation is required) to an amplifier which has a low impedance voltage output (SL680C and SL1680C) and a current output from a free collector (SL680C only). The amplifier output is fed back via an attenuator to the base of the common-emitter amplifier, and the attenuator is controlled by a level signal derived via a detector from the output stage. This arrangement ensures constant output irrespective of crystal activity. The circuit also contains a supply voltage regulator.

The SL680C has very low crystal drive, of the order of 50nW per ohm of ESR and thus contributes very little to the ageing of the crystal with which it is

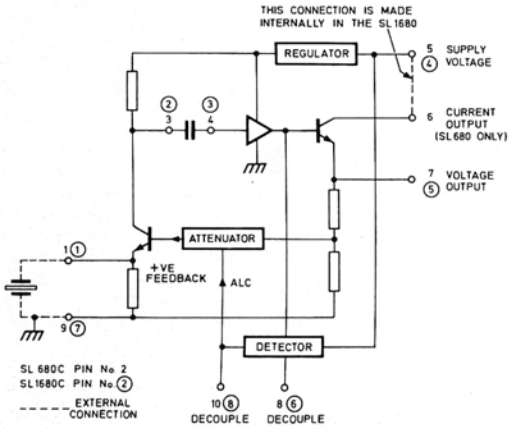


Fig. 34 Block diagram of SL680C

used. Its phase shift variation with temperature and supply variation is also so low as to be insignificant as a factor in oscillator frequency variation. Such features are valuable where stability and good ageing characteristics are required, but are achieved at the cost of a base-band noise level of —85dB with respect to carrier in a 1Hz bandwidth.

CIRCUIT APPLICATIONS

The crystal is connected between pin 1 and ground. Pin 1 has a DC potential of about 3.5V but crystal dissipation is only 50R nW, where R is the crystal ESR in ohms. For most crystals this results in a dissipation of between 0.5 and 1 microwatt.

The SL680C supply should be decoupled to ground at HF with a low RF impedance capacitor of about 0.1 microfarad. There are two internal points, one each in the detector and attenuator, which must also be decoupled by good RF capacitors of around 0.01 to 0.1 microfarad. Early versions of the SL680C (but not the SL1680C) also required decoupling of pin 2, a point in the voltage regulator. This decoupling is no longer necessary and in SL680C devices manufactured since the beginning of 1977 (datecode 7700 onwards) no connection is made from the chip to pin 2.

The output of the common-emitter amplifier at pin 3(2) has an impedance of 500 ohms. When the circuit is used as a fundamental oscillator the two pins may be connected together by a capacitor of about 500pF and for third overtone oscillation with a capacitor of a few tens of picofarads (the particular value depending on the frequency required). Some crystals will oscillate in the third overtone even when fundamental operation is required; in this case pin 4(3) should be decoupled to ground with a capacitor having a reactance of 50 ohms at the unwanted overtone frequency.

For operation at higher overtones a tuned circuit is necessary between pins 3(2) and 4(3) with a tap to match the 50 ohm impedance. With such a tuned circuit it is possible to make crystals oscillate at their seventh, ninth or even eleventh overtones.

At low frequencies (about 150kHz) oscillators using the SL680 start very slowly. A delay of up to 10 seconds may occur between the initial application of power and the commencement of oscillation.

The SL680 has two outputs, voltage and current; the SL1680 has only a voltage output. The current output pin consists of a free collector, which must be biased to the positive supply via a load which may be resistive, inductive, or a tuned circuit. The standing current in the collector is about 1.2mA and the signal is 350 microamps rms. If the current output pin is not required it must be connected to the positive supply. When it is used its load must be such that it never drops below +2.5V.

The voltage output has an amplitude of about 150mV rms and will drive impedances as low as 100 ohms (or even 50 ohms if an external load resistor of 470 ohms is connected from the output pin to ground). The output signal must be coupled to its load by a capacitor to preserve the DC conditions of the output stage.

Both outputs consist of sinewaves with harmonic content typically less than 1 per cent. To drive logic such as TTL or CMOS from the SL680C requires buffer circuitry. As an alternative, the Plessey SP705B oscillator maintaining circuit might be used in logic driving applications since it has TTL compatible outputs.

SP8000 series

High speed dividers

The SP8000 Series is a range of high speed digital dividers using ECL techniques. Devices with division ratios from ÷2 to ÷256 are available and some types operate at frequencies up to 1.5GHz. To describe the various types in full is outside the scope of this book. However, since high speed dividers have numerous applications in radio systems, a brief description of the range and some notes on applications for the circuits will be given.

CIRCUIT DESCRIPTIONS

Table1a summarises the SP8000 range of fixed modulus dividers (i.e. those which divide by a single ratio) and Table1b summarises the two-modulus programmable dividers (i.e. those dividing by N or N + 1 depending on the state of a control input). It will be seen that there are a wide number of division ratios and input/output interfaces but all the devices in the SP8000 range use emitter coupled logic (ECL) chip circuitry.

The signal inputs of SP8000 devices can be differential or single-ended and DC or AC coupled depending on the particular device. Signal is supplied to AC coupled devices via an isolating capacitor (usually about 1000pF) but DC coupled devices have no internal bias circuitry and may be driven either from ECL II or ECL III or be driven with AC via a capacitor and biased by a separate external resistor network.

The datasheet for each device states which of the two ECL families is appropriate and also describes the bias network. Devices with balanced inputs may be driven with a differential signal, or a single signal may be applied to one input and the other decoupled to ground by a 1000pF capacitor.

If no signal is applied to a balanced input the device will tend to oscillate at some ill-defined but high frequency. This may be prevented by applying a bias to one of the inputs by means of a resistor connected from the input to one or other of the supplies. This has the effect of desensitising the input but preventing oscillation – the exact value of the resistor depends on the device used but is generally around 10 kilohms. SP8000 series devices will operate with sinewave inputs at high frequencies but low frequency sine inputs may cause malfunction.

Counters specified to have maximum operating frequencies of 700MHz or more should not be used with sine inputs under 80MHz. At frequencies lower than this they should be driven with square wave inputs having rise and fall rates in excess of 200V/microsecond. Lower frequency counters may be used with sine inputs down to 40MHz and then with square waves with 100 microsecond rise and fall times. Some SP8000 circuits are less demanding – details are given in their respective data sheets.

The input signal required by SP8000 series circuits for satisfactory operation is between 400 and 800mV peak-to-peak except in the case of one or two of the very high speed counters which require a minimum of 600mV. Many counters will operate with inputs well outside this range but it is unwise to allow them to do so as the circuit configurations used in the counters can lead to miscounting at certain frequencies if too high or too low an input level is used.

Type	Max. Freq. (MHz)	Div. Ratio	Input	Output	Power mW(V)
SP8000	250	4	Balanced DC	Balanced free collector	85
SP8601	150	4	Balanced DC	Balanced free collector	85
SP8602	500	2	Balanced AC	Balanced emitter follower	60
SP8603	400	2	Balanced AC	Balanced emitter follower	60
SP8604	300	2	Balanced AC	Balanced emitter follower	60
SP8607	600	2	Balanced AC	Balanced emitter follower	70
SP8613	700	4	AC	Balanced ECLII	330(7.4)
SP8614	800	4	AC	Balanced ECLII	330(7.4)
SP8615	900	4	AC	Balanced ECLII	330(7.4)
SP8616	1000	4	AC	Balanced ECLII	330(7.4)
SP8617	1300	4	AC	Balanced ECLIII/10K	550(6.8)
SP8619	1500	4	AC	Balanced ECLIII/10K	550(6.8)
SP8620	400	5	AC	ECLII	300
SP8621	300	5	AC	ECLII	300
SP8622	200	5	AC	ECLII	300
SP8628	150	100	Balanced AC	TTL	170
SP8629	150	100	Balanced AC	TTL	170
SP8630	600	10	AC	Emitter follower	360
SP8631	500	10	AC	Emitter follower	360
SP8632	400	10	AC	Emitter follower	360
SP8634	700	10	AC	TTL(BCD)	400
SP8635	600	10	AC	TTL(BCD)	400
SP8636	500	10	AC	TTL(BCD)	400
SP8637	400	10	AC	TTL(BCD)	400
SP8650	600	16	Balanced AC	Balanced ECLII	230
SP8651	500	16	Balanced AC	Balanced ECLII	230
SP8652	400	16	Balanced AC	Balanced ECLII	230
SP8655	200	32	Balanced AC	Free collector	55
SP8657	200	20	Balanced AC	Free collector	55
SP8658	200	20	Balanced AC	Free collector	100
SP8659	200	16	Balanced AC	Free collector	55
SP8660	180	10	Balanced AC	Free collector	55
SP8665	1000	10	AC	ECLII	550(6.8)
SP8666	1100	10	AC	ECLII	550(6.8)
SP8667	1200	10	AC	ECLII	550(6.8)
SP8670	600	8	Balanced AC	Balanced ECLII	230
SP8671	500	8	Balanced AC	Balanced ECLII	230
SP8672	400	8	Balanced AC	Balanced ECLII	230
SP8675	1000	8	AC	ECLII	475(6.8)
SP8676	1100	8	AC	ECLII	475(6.8)
SP8677	1200	8	AC	ECLII	475(6.8)
SP8735	600	8	AC	TTL (1-2-4 binary)	360
SP8736	500	8	AC	TTL (1-2-4 binary)	360
SP8750	1000	64	AC	TTL	450(6.8)
SP8751	1100	64	AC	TTL	450(6.8)
SP8752	1200	64	AC	TTL	450(6.8)
SP8770	1200	256	AC	TTL	450(6.8)

Table 1a SP8000 series high speed dividers

Type	Max. Freq. (MHz)	Div. Ratio	Input	Output	Power mW(V)
SP8640	200	10/11	ECLIII/10K	Balanced ECLII	260
SP8641	250	10/11	ECLIII/10K	Balanced ECLII	260
SP8642	300	10/11	ECLIII/10K	Balanced ECLII	260
SP8643	350	10/11	ECLIII/10K	Balanced ECLII	260
SP8646	200	10/11	ECLIII/10K	Balanced ECLII and TTL	260
SP8647	250	10/11	ECLIII/10K	Balanced ECLII and TTL	260
SP8685	500	10/11	AC	Balanced ECLII	230
SP8690	200	10/11	Balanced AC	Balanced ECLII and free C	75
SP8695	200	10/11	ECLIII/10K	Balanced ECLII and free C	85
SP8740	300	5/6	AC	Balanced ECLII	230
SP9741	300	6/7	AC	Balanced ECLII	230
SP8743	500	8/9	AC	Balanced ECLII	230
SP8745	300	5/6	ECLIII/10K	Balanced ECLII	250
SP8746	300	6/7	ECLIII/10K	Balanced ECLII	250
SP8748	300	8/9	ECLIII/10K	Balanced ECLII	250

Table 1b SP8000 series two-modulus prescalers

The control inputs of the two-modulus counters are ECL-compatible.

The majority of SP8000 outputs are emitter followers, usually ECL-compatible, but some of the series have free collector or TTL compatible outputs. Many of the devices have both Q and Q and some of the decades have BCD outputs.

No particular problems arise in the output circuitry although the emitter follower outputs should not be used to drive capacitive loads.

The SP8000 series circuits require 5.2V supplies except a few of the faster circuits, which require higher voltages such as 6.8V or 7.4V. The data sheets suggest the use of positive ground supplies; this has the advantage of minimising the risk of damage due to output short circuits but can be inconvenient if the counters are to be used in conjunction with other integrated circuits using the more conventional negative ground. But whether positive or negative ground is used it is most important that the power supplies be adequately decoupled. Quite small capacitors may be used — 100pF is more than ample and in some applications as little as 15pF has been shown to be sufficient.

The capacitors used must, however, be RF types having minimal lead and package inductance. The capacitors should be sited as close to the integrated circuits as possible and leads kept short. It is not use ensuring that a capacitor lead is short if the printed track to it is long and thin — board tracks must also be kept short and as wide as possible. A ground plane on one side of the circuit board with all ground connections made to it minimises lead inductance problems and is the best way to ensure satisfactory operation of any high speed or high frequency circuitry.

Similar care to that spent on decoupling should be lavished on the bias points in the circuit and the unused inputs. Capacitors need not be particularly large but must have good high frequency performances and very short leads

and tracks. It is impossible to emphasis too much the importance of good practice in grounding and decoupling circuits such as the SP8000 series — over two thirds of all the applications problems referred back to the Plessey Applications Laboratory concerning these circuits arise from lack of such practice.

MODULUS EXTENDERS FOR TWO-MODULUS DIVIDERS THE SP8790 AND SP8794

The SP8790 and the SP8794 are designed for use with two-modulus dividers to extend their division ratios and hence make them more suitable for use with CMOS and low power TTL. The SP8790 converts a $\div N/N+1$ counter to a $\div 4N/4N+1$ counter and the SP8794 converts it into a $\div 8N/8N+1$ counter.

Each device consists of a counter with a balanced AC-coupled input, a CMOS or TTL compatible output, and a control output designed to drive the control inputs of the SP8000 series of two-modulus dividers. There is also a control input which is CMOS or TTL compatible (but needs a 5 kilohm pullup resistor when used with TTL).

In use, the control input from the programmable divider goes to the control input of the SP8790 (or the SP8794) and is gated to the two-modulus divider once every four (or eight) counts. Fig. 35 shows an SP8790 used with an SP8695 to give a $\div 40/41$ counter; similar systems may be used with any of the SP8000 two-modulus dividers.

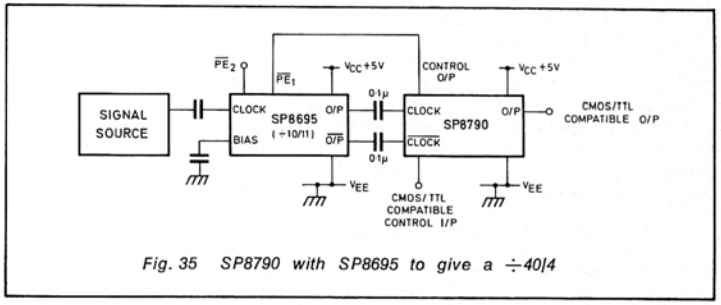


Fig. 35 SP8790 with SP8695 to give a ÷40/4

The SP8790 and SP8794 will normally be driven by SP8000 high speed dividers which have fast output edges. If other sources are used, however, the notes on input waveform slew rate in the preceding section should be observed. Again, the input should be biased if there is likelihood of instability in the absence of a signal, and the unused input should be decoupled to ground if only one input is required. The input level should be between 300mV and 1V peak-to-peak.

The internal delays in the SP8790 and the SP8794 do not allow their operation at input frequencies (to the SP8790 or SP8794) of over 40MHz as a controller. However, if the SP8790 or SP8794 are used as simple dividers they will work at over 60MHz and 120MHz respectively.

Both devices require a single 5V supply which must, as usual, be well decoupled. Neither device has any other points which need to be decoupled with the possible exception of unused inputs.

SP8760

General purpose synthesiser

The SP8760 is a general-purpose circuit intended for use in conjunction with CMOS or TTL programmable counters, and with high speed prescalers, in frequency synthesisers. It consists of a crystal oscillator with two-stage divider, a ÷15/16 two-modulus counter, and a high performance type II phase/frequency comparator. All three sections of the device have CMOS/TTL interfaces and the phase/frequency comparator offers better zero error and phase jitter characteristics than other such integrated circuits.

CIRCUIT DESCRIPTION (Fig. 36)

The crystal oscillator uses an emitter-coupled circuit with a series resonant crystal connected between pins 4 and 5. It is internally rolled off to prevent overtone operation and will not work at frequencies much above 10MHz. This oscillator has a series resonant crystal and has a stability of about 0.2ppm/degree C, excluding the crystal itself.

If the divider is required but not the crystal oscillator, an external signal may be applied to pin 4 via a small capacitor in series with 220 ohms. Pin 5 may, in that case, either be decoupled or left open depending on the frequency and amplitude of the signal on pin 4.

The output of the oscillator is not available externally but only via a ÷4 circuit. This circuit, like the rest of the logic interfaces on the SP8760, has a CMOS/TTL compatible output, which is connected to pin 11.

The two-modulus divider (÷15/16) has a CMOS/TTL clock input on pin 6 and its output appears on pin 9. When the control input, pin 8, is high the divider divides by 16 and when it is low it divides by 15. The standard TTL fan-in of the clock input is 1 and the output fan-out is 3.

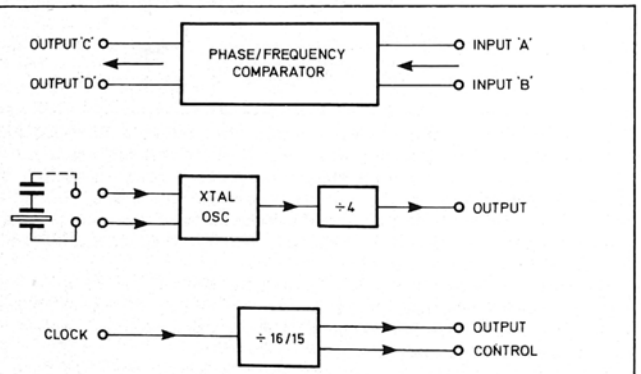


Fig. 36 SP8760 block diagram

The maximum clock frequency of the SP8760 is at least 12MHz (typically 18MHz). Hence the use of almost any family of low speed logic is permissible in the main divider of a synthesiser using the SP8760 since its output will never exceed 1MHz under proper operation.

The comparator has an infinite pull-in range (subject, of course, to an input frequency response of about 10MHz) and zero phase shift at phase-lock. The comparator pulse width at zero phase shift is under 30ns, giving minimum noise and jitter.

In operation the comparator triggers on the 1 to 0 transition of each input and gives outputs on pins 1 and 2 proportional to the phase difference between the two transitions. When the edge on pin 14 occurs before the edge on pin 13 the output on pin 1 will be low during the interval between the two transitions and the output on pin 2 will remain low whereas if the edge on pin 14 occurs after the edge on pin 13 the output on pin 2 will be high between the two transitions and pin 1 will remain high. The decision as to which is the 'first' transition is made by counting pulses at each input — if two pulses occur at one input without any ocurring at the other the second of the two is considered to be the 'first' and the relevant output changes state until a 1 to 0 transition occurs on the other input. Once an input has counted two in this way it remains the 'first' input until two transitions occur on the other input without one ocurring on it, when the other input becomes the 'first' input. The SP8760 phase comparator timing diagram is shown in Fig. 37.

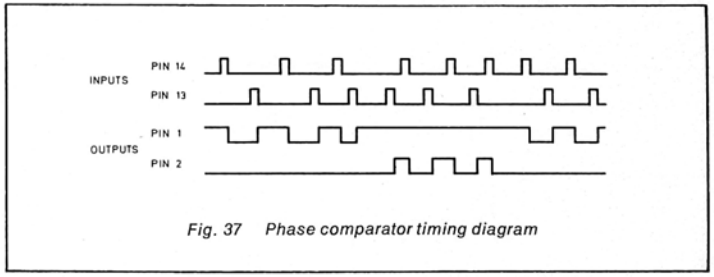


Fig. 37 Phase comparator timing diagram

The output on pin 1 consists of the collector of an NPN transistor with a 10 kilohm resistor to V_{ee}. Three ways of driving the varactor line of a voltage controlled oscillator from these outputs are shown in Fig. 38. The simplest way, shown in Fig. 38(a), is only suitable for use when the varactor voltage change is very small — say, less than 1V from 2 to 3V. The low voltage charge pump in Fig. 38(b) can be used with varactor voltages between 1V and 4V and the high voltage charge pump in Fig. 38(c) is used where large varactor voltage swings are necessary. The transistors and diodes used in these circuits should be silicon types with a fast switching speed to avoid degrading the performance of the phase comparator. The transistors used in the circuit in Fig. 38(c) need also a V_{ceo} of at least 35V.

The leakage on the varactor line must be as low as possible since any leakage leads to jitter as the charge pump replaces the lost charge. A high impedance buffer may be placed between the output of the charge pump and the varactor line and indeed is essential if varactor line losses are high.

Since noise in this buffer will itself cause oscillator jitter, it is better to use a non-leaky varactor line and no buffer if at all possible.

The SP8760 uses a single 5V supply, which must be well decoupled at HF and LF and draw about 45mA.

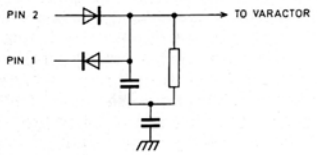


Fig. 38a Simple charge pump

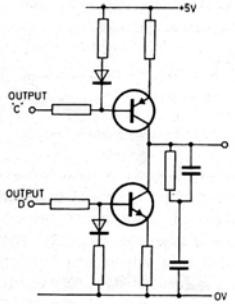


Fig. 38b Low voltage charge pump and filter. Divider clock input

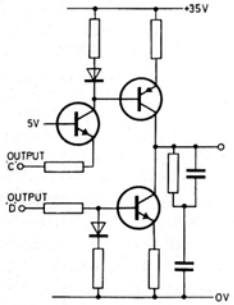


Fig. 38c High voltage charge pump and filter

SP8921 series

Synthesisers for CB radio

The SP8921 series is a range of circuits designed for use in 27MHz Citizens Band synthesisers. Each synthesiser consists of two chips and a dozen or so external components. One chip contains a crystal oscillator at 10.240MHz (using an external crystal) and a 2^{13} divider, a phase/frequency comparator (similar to the one in the SP8760) and a counter with programming capability: the second chip contains an ECL prescaler and the main programmable counter.

Three pairs of circuits are available. The SP8921/SP8922 combination synthesises 128 channels at 5kHz intervals, starting at 26.895MHz, and the same channels with offsets of —455kHz, —10.240MHz, or —10.695MHz. These offsets are programmed on two pins, one on the SP8921 and one on the SP8922. The channels are programmed by seven pins on the SP8922. The SP8926/SP8927 combination performs the same function as the SP8921 and SP8922 except that the offsets are +455kHz, +10.240MHz, or +10.695MHz. When 26.895MHz is programmed it is not possible to use any of the offset functions with either of the above pairs of devices, so only 127 channels are available with offsets.

The SP8931/SP8932 combination differs from the other two pairs of circuits in that they do not program the basic frequencies at all, but program with offsets of ±455kHz, ±10.240MHz, or ±10.695MHz. Since these chips do not program the basic frequencies only 127 channels are available with any particular offset.

Package connections are shown in Fig. 39. It will be seen that the SP8921, the SP8926, and the SP8931 have identical pinning, as have the SP8922, the SP8927 and the SP8932.

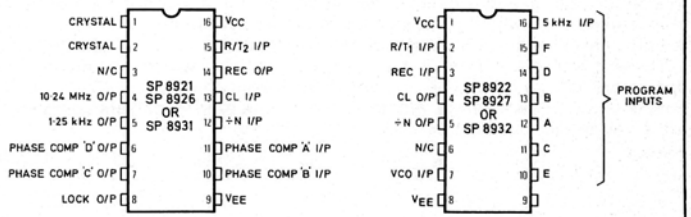


Fig. 39 Pin connections (top view)

All the inputs to these circuits with the single exception of the input to the ECL prescaler are shown in Fig. 40, a simple RTL input. The ECL prescaler has a self-biased input; the input to it should be between 400mV and 1V rms and should be coupled through a capacitor. All the logic outputs are of RTL type and have collector loads of 5 kilohms except the lock indicator which has a load of 10 kilohms.

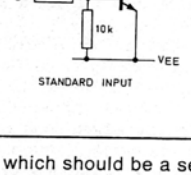


Fig. 40 Standard input of SP8921/22

The crystal, which should be a series resonant type, is connected between two emitters, each having a resistance to ground of 3.5 kilohms. If an external oscillator is required, a signal of a few hundred millivolts rms should be applied via a capacitor to one of the crystal pins and the other left unconnected or decoupled. Whether or not to use decoupling depends on the amplitude of the signal input. Decoupling can sometimes cause instability so should not be undertaken 'just in case'.

There is an output at the crystal frequency on pin 4 of the SL8921/26/31. This output is rather rich in harmonics and has an amplitude of about 700mV p-p. If a clean sine wave of about 200mV is required a 4.7 kilohm resistor may be connected from pin 4 to low Q tuned circuit formed by a parallel inductor/capacitor.

The phase/frequency comparator is very similar to the one in the SP8760 described in the previous section but does not have 10 kilohm pullup and pulldown resistors. The same charge pump arrangements may therefore be used, but the diodes are not necessary in the first of the three. An addition to this comparator is a lock detector circuit, the output of which is high when the loop is locked but which generates a stream of negative pulses when the loop is unlocked. This pulse stream can be smoothed and used to indicate lock.

These circuits run from a single 5 volt supply, which should be well decoupled at both HF and LF and each circuit consumes about 45mA. Further details of the SP8921 series, and the descriptions of synthesisers using them, are given in the following section.

Section 2

System designs

Receiver systems

THE SYNCHRODYNE

The simplest receiver that can be built from SL600 devices is the Synchrodyne, an example of which is shown in Fig.41a. Such direct conversion receivers may be used for the demodulation of SSB, AM and DSB, where the VFO is tuned to the carrier frequency (for AM and DSB the VFO must be phase-locked to the carrier). For CW reception, the VFO is tuned a few hundred Hertz away from the carrier, resulting in an audible beat with the CW. Upper and lower sidebands are equally well detected by this receiver, which can be very selective if the audio passband is limited. If, however, a Synchrodyne is used to receive, say, an upper sideband SSB signal with a carrier frequency f kHz, then another such signal with carrier frequency lying between f and (f — 3) kHz will, if present, be detected (though not intelligibly) and cause interference. The interference can be removed, and one sideband only detected, by use of the phasing system shown in Fig. 42.

The system in Fig. 41a is, of course, only a detector; as such it is not very sensitive and has no AGC. A more complete system, illustrated in Fig. 41b, has RF filters to minimise cross-modulation, an RF amplifier (or RF amplifiers), AGC and an optional 'S' meter. Whether one or two RF amplifiers are used will depend on the sensitivity required and the AF gain available; these factors, together with considerations of operating frequency, will determine the choice of device from the SL610C, SL611C and SL612C range. The SL612C has the additional advantage of a lower current consumption and slightly lower noise figure.

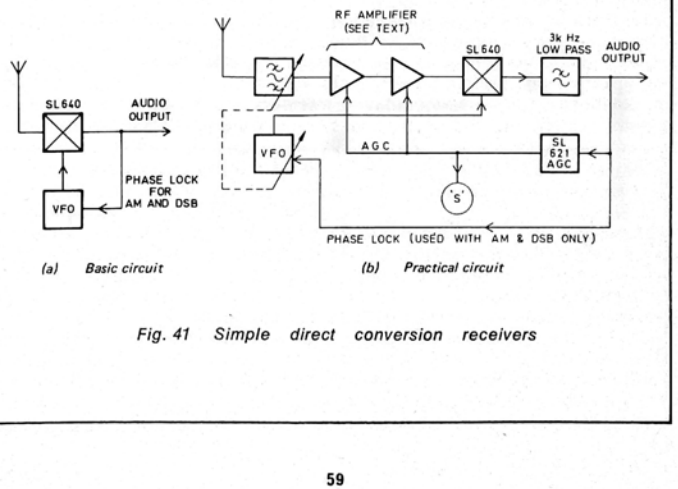


Fig. 41 Simple direct conversion receivers

Fig. 42 shows a more complex direct conversion receiver which employs RF and AF phasing to cancel one sideband so that it is a truly single sideband receiver. It is necessary to have accurate phasing of the signals and well-matched gain in the two audio channels before the summing stage. Upper or or lower sideband may be selected by reversing the phasing of the RF or, for simplicity, the audio signal. The system illustrated detects LSB when the upper channel is in phase, USB when it is out of phase by — 90 degrees.

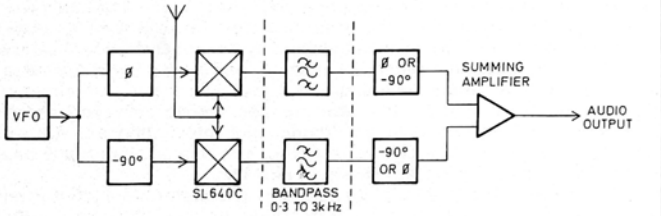


Fig. 42 SSB direct conversion receiver

THE CONVENTIONAL SUPERHET

A basic superhet is shown in Fig. 43. The signal from the antenna, having passed through a preselector filter, is amplified and then mixed with a local oscillator to produce an intermediate frequency. This IF signal is filtered to remove signals on adjacent channels, amplified to a detector. An AGC voltage is fed back to the RF and IF amplifiers.

This system has been in use, first with valves and distributed IF amplifiers — later with transistors and/or block crystal filters — since the late 1920s. In many respects it is ideal — it has high gain, low noise and excellent selectivity. Many of the most famous receivers of the past used such a system but it has one severe drawback — the large gain in the relatively broadband stages prior to the IF filter can lead to large unwanted signals being applied to the mixer which in turn (and especially with transistor mixers) leads to cross-modulation. Once cross-modulation has occurred no amount of subsequent filtering will cure it. The problem was less severe in the past for two reasons

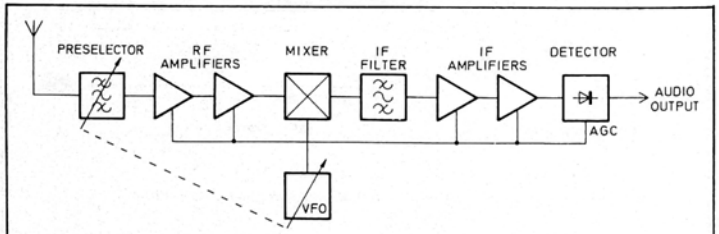


Fig. 43 The traditional basic superhet

— the valve mixer is far less susceptible to such effects, and, far more important, in the past there were far fewer strong signals liable to cause such troubles than there are on today's crowded spectrum.

Modern receiver design has moved away from such techniques. The design of HF and VHF receiver front ends is a difficult task and the systems used in the highest performance receivers are often complex. In principle, however, two criteria must be considered — firstly, a minimum of gain between the antenna and the crystal filter (usually none at HF where antenna noise levels are high but possibly 10dB at VHF and UHF so that mixer noise does not control system sensitivity; in mobile radios at VHF/UHF, however, sensitivity is often sacrificed for strong-signal performance) and, secondly, the use of a mixer having as great a cross-modulation resistance as possible. Some common mixers are discussed below.

The bipolar transistor is a very poor mixer and suffers badly from cross-modulation. Its common use in television tuners is responsible for their extreme susceptibility to cross-modulation by local transmitters. However, the use of bipolar transistors in the microwave region can give some cost advantages over other systems. Junction FETs, although far better for the purpose than bipolar transistors, do not make ideal mixers when used alone.

Cross-modulation resistance can be greatly improved by employing bipolar transistors in double-balanced modulator circuits such as the SL640 or SL641. The SL640/1 will tolerate up to 30mV rms of unwanted signal before cross-modulation of a 1 microvolt signal reaches 1 percent. This is not a very good performance by the standards of modern HF receivers; nevertheless the SL640/1C may be used in medium performance receivers where its low local oscillator power requirement and extreme ease of use in some degree compensate for its less than ideal large signal performance. It should be noted that if the SL640/1C be preceded by an SL610C to which no AGC is applied the signal at the antenna needed to produce cross-modulation is reduced from 30mV to 3mV. This is not satisfactory.

A single balanced modulator using a matched pair of junction FETs can have useful gain, low noise, and high cross-modulation resistance, but has one disadvantage in that quite high local oscillator power is required. Nevertheless, it has been demonstrated that a mixer with 2.5dB gain, working from 50MHz to 300MHz and capable of handling signals in excess of 2V rms can be made using this technique.

The dual-gate MOSFET is another, useful mixer. The fact that it is more often used at VHF than at HF appears to result more from custom than for any real technical reason. It will handle signals of over 150mV but its biasing is somewhat critical. Local oscillator requirements, however, are modest and it can have both useful gain and low noise figure.

Of all the mixers in use today, however, the diode ring is undoubtedly the best. Using four matched diodes of any type (most commonly used are silicon Schottky diodes and, in low-cost systems, germanium diodes), this mixer has many advantages. It is bi-directional (so that it may be permanently connected to the filter of any transceiver and yet be used on both transmit and receive (see Fig. 41), it will suppress very large unwanted signals — although this is also dependent on the local oscillator power inserted — and can be used at frequencies up to several GHz. Disadvantages of the diode ring mixer are its high local oscillator requirement, its conversion loss of about 6dB and its noise figure of 5dB or more. Several manufacturers make silicon Schottky

diode rings with very broadband 50 ohm ports at quite reasonable prices. These are used wherever diode ring mixers are specified in this application note.

The mixer, therefore, and any RF amplification preceding it, must be as resistant as possible to cross-modulation. It may be noted that while an SL640/1 can only tolerate 30mV rms of unwanted signal, an SL610C without AGC will accept 100mV — but a mixer capable of handling 1V would have to follow it. Using an SL610C with full AGC cross-modulation is encountered at about 250mV rms input. The mixer must be followed at once by the filter. In modern sets a crystal or ceramic filter is usually employed, so no other type will be considered here. The bandwidth of the filter depends on the signal being received — bandwidths commonly used are given in Table 2.

Signal Mode	BW (kHz)
CW (morse code)	0.3 — 0.6
SSB	2.7
AM (Voice)	5.5
NBFM	6 — 25 *

*This depends on how NB the FM is

Table 2

The filter is followed by a high gain broadband IF amplifier consisting of two or three SL612Cs followed in turn by a detector, AGC generator and the audio stages.

AN SSB RECEIVER

A receiver as outlined above is described in detail in Section 3 as the receiver section of an SSB transceiver. Its circuit diagram is given in Fig. 44. It consists of a diode ring mixer fed from the antenna via a preselector followed by a crystal filter (an SEI QC1246 AX 2.4kHz bandwidth 9MHz filter was used in the prototype) and a 3-stage SL612C IF amplifier. An SL640C acts as product detector and feeds an SL621C AGC generator and an SL630C audio amplifier.

The AGC line is decoupled to keep RF from the AGC inputs of the SL612Cs but too large a value of decoupling capacitor degrades the impulse interference suppression characteristics of the SL621C. This type of suppression, while not as effective as a full noise-blanking circuit, nevertheless reduces impulse interference to an acceptably low level for most receivers. A suitable total capacitance on the AGC line is 15nF. The resistor in the AGC line of the first SL612C may be larger than the resistors in the AGC lines of the other two devices; alternatively a silicon diode could replace the resistor. Either of these techniques will ensure that the first SL612C remains at full gain for a while after the detector output has passed the AGC threshold, thus maintaining a high signal-to-noise ratio.

The supply line is decoupled at LF to prevent supply current surges (which

in the SL621C can be induced by step signals) from interfering with other circuits. The SL612Cs have internal decoupling, but it is advisable to earth the cans to pin 8. The interstage IF coupling capacitors should be kept as small as possible — at 9MHz 100pF is adequate — to ensure that LF signals at the output of one SL612C (due to noise or AGC action) do not reach the next stage and give rise to low frequency instability as the receiver passes the AGC threshold.

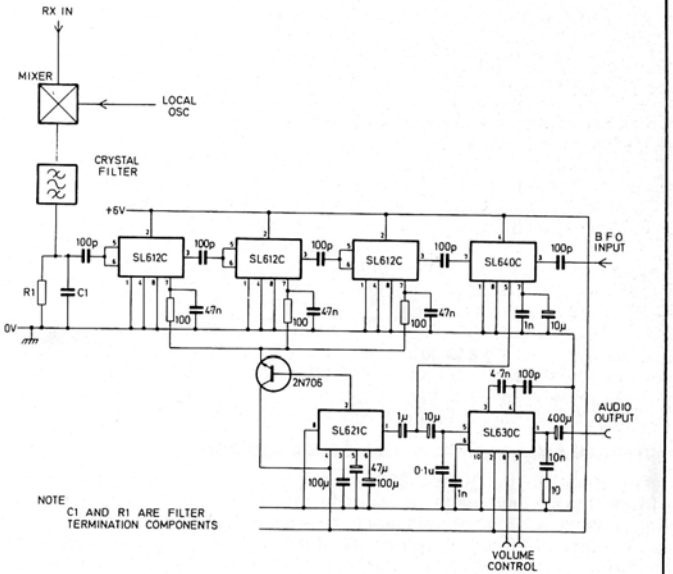


Fig. 44 SSB receiver circuit diagram

Earlier designs of SL600 SSB receivers using SL600 devices had a preset control to adjust the AGC threshold. This is now considered unnecessary. The audio output from the receiver is a maximum of 100mW which, while entirely adequate for headphone and normal domestic or fixed amateur use, may be insufficient for mobile or professional applications (although a listening test is worthwhile here, as 100mW is louder than most people imagine). If more output is needed, however, an extra power amplifier may be mounted off the board.

The circuit board described uses single-sided copper board. The layout is extremely critical and deviations from it are likely to lead to instability. If a different layout is used it would be better to use double-sided board and make all earth connections to a continuous unetched earth plane on the component side of the board. If a new or different design is attempted on single-sided board, strict attention must be paid to the instructions on earth connection given in the SL610/11/12 circuit data.

FM RECEIVERS

Land Mobile Radios

In the VHF or UHF, bands land mobiles use narrow deviation FM (Δf between 1.5 and 12kHz) and generally use a first IF of 10.7 or 21.4 MHz. The SL664C and the SL665C are ideal for use in such receivers. The SL664C, which has a standby power drain of only 20mW and can drive a loudspeaker with up to 250mW, is ideally suited for use in hand-held transceivers while the SL665C, which has slightly greater standby power and does not contain a power audio output stage, is better suited for use in mobiles. Both circuits have a sensitivity of better than 10 microvolts and use quadrature detectors optimised to give excellent S/N ratios when working with narrow deviation signals at 10.7 or 21.4 MHz IF. Traditional quadrature circuits were designed for consumer applications such as television and broadcast FM which use deviations of up to 75KHz and they are quite unsuitable for use with narrow deviation signals because of the damping effect of their quadrature port impedance on the LC quadrature circuits used with them. The SL664C and SL665C have been designed to avoid this problem.

The SL664C and SL665C also contain a squelch system using carrier detection and having 2 to 3dB hysteresis. The squelch in the SL664C turns the detector and the audio stages on and off to conserve power but the one in the SL665C merely drives a flag output and the detector works all the time – allowing the SL665C to be used with tone squelch systems.

Broadcast FM Receiver and TV Sound Systems.

These can use the SL664C/665C merely by using a quadrature element with a lower Q to accommodate the wider deviation. The circuit alteration can be as simple as the addition of a resistor between pins 4 and 5 to load the quadrature coil – although the prime selectivity of the receiver must be suitable for the bandwidth of the new type of signal. The SL664C is particularly useful in portable FM receivers in that it will supply adequate power to a loudspeaker but consumes only a few milliamperes, prolonging battery life.

MULTIMODE RECEIVERS

In multimode receivers, different filter bandwidths are required for different modes. An ideal multimode receiver would contain an IF filter which could be adjusted in bandwidth from a few hundred hertz (for slow CW signals in a noisy environment) to several hundred kilohertz (for entertainment grade wide FM). Such systems are possible but the techniques used to produce infinitely variable passbands are complex and expensive and outside the scope of this book.

A very simple multimode receiver might use a single filter wide enough to accommodate the widest type of signal to be received but this would generally

give unacceptable results on the other modes. The remaining solution is to use a number of filters corresponding to the principal modes to be received.

For an inexpensive receiver two filters might be sufficient — one of 2.7kHz bandwidth for CW, SSB and AM (assuming that the loss of one sideband during AM reception is acceptable) and one of about 12kHz bandwidth for narrow FM.

For a more expensive receiver four or even more filters might be used with (say) 500Hz, 2.7kHz, 6kHz, 12kHz and perhaps other bandwidths.

A good quality crystal filter of 8 or 10 poles will have a stopband attenuation of over 90dB. It is necessary to take care when switching such filters to prevent degradation of the stopband attenuation due to coupling between input and output switch sections. Sometimes the problem is overcome by using the widest bandwidth filter on all modes, with broadband IF gain, followed by switched 4- or 6-pole filters to define the final IF bandwidth. This system does not have quite such good strong signal performance as others since signals within the passband of the wide filter, but out of the passband of the selected filter, can overload the first broadband IF stage.

Another solution is to buffer the mixer to all four filters and have separate IF strips for each mode. Switching is then accomplished by applying power to the appropriate IF strip. This multi-strip technique has much to recommend it since each strip can use the best possible detector and AGC system for the mode in use but it generally uses more parts than a receiver with common sections and hence costs more.

The receiver section of the multimode transceiver described in section 3 uses a combination of two techniques: separate IF strips and cascaded filters. The buffer following the mixer drives two filters, one of 12kHz wide that drives the FM IF strip and one of 2.7kHz wide that is followed, after some IF gain, by switched filters of either 2.7kHz (for AM and SSB) or 500Hz (for CW) bandwidth.

Figs. 45 and 46 show the cascaded filter and multiple IF strip techniques respectively.

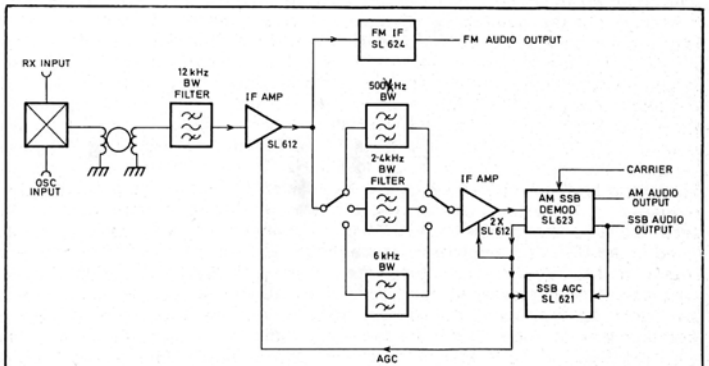


Fig. 45 AM/SSB receiver block diagram

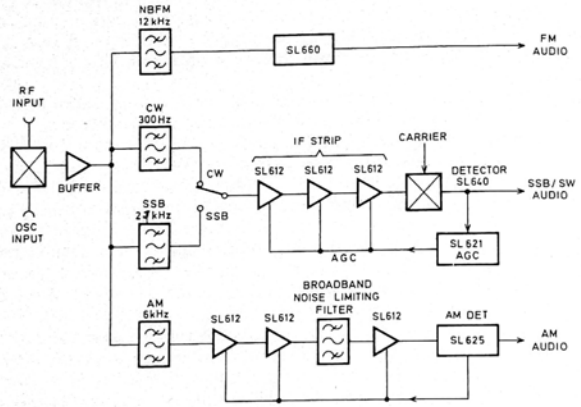


Fig. 46 Multimode receiver using separate filters and IF strips

DOUBLE SUPERHETS

In the absence of crystal filters it is difficult to design an IF strip having narrow bandwidth and a high enough IF to overcome image problems. One solution is to have two IFs — one high to overcome image problems and the other low with a narrow bandwidth. In the early days of radio this technique was common and most good HF receivers were double or even triple superhets.

Today with the availability of excellent crystal filters, double superhets are unnecessary at HF or VHF, as excellent receivers are possible with a single IF. Double conversion receivers are still used however, where they can simplify sophisticated tuning arrangements or where they contribute to cost reduction. For example synthesised HF receivers usually use a first IF above their 0 to 30MHz tuning range so that their local oscillator can use a single octave VCO. Generally the first IF is about 35MHz, necessitating a tuning range in the local oscillator of 35 to 65MHz. There is then a second conversion to an IF which can be as low as 455kHz without image problems. An example of a system where cost constraints dictate double conversion techniques is the inexpensive 27MHz 40-channel Citizens' Band receiver used in the USA and elsewhere. Since these sets sell for as little as $79 it is impractical to use a crystal filter in their IF which leaves only ceramic filters with adequate selectivity for the 10kHz channels in use. Such ceramic filters can only be manufactured with sufficiently narrow bandwidth at centre frequencies of around 455kHz. However it is difficult to make a single conversion receiver having a first IF of 455kHz and sufficient image rejection at 27MHz. The solution is to use double conversion with a first IF of about 10.7MHz. At that frequency a ceramic filter costs only a few pence but has

about 200kHz bandwidth for IF tuning. In early CB radios, before the introduction of integrated circuit synthesisers, the use of switch-tuned crystal-controlled local oscillators for both the first and second conversions simplified the design of multi-channel receivers and used fewer quartz crystals.

SL600 series devices can of course be used in double superhets. The circuit techniques used are almost identical to those in single conversion receivers but care is necessary to avoid excessive gain, particularly before the main filter.

Transmitter systems

FILTER TYPE SSB EXCITERS

Two types of SSB generator are in common use: filter systems and phasing systems. A basic filter system is shown in Fig. 47. The audio and a low radio frequency from an oscillator (the BFO if the system is part of a transceiver) are mixed in an SL640C which, as a result of its good carrier rejection, gives as its output a clean DSB suppressed-carrier signal. This is passed through a narrow bandpass filter to remove one sideband, the remaining sideband is converted to the final frequency by another SL640C and the image is removed by a filter. The output is then applied to the transmitter linear amplifier, possibly using a Plessey Semiconductors SL560C as its first stage.

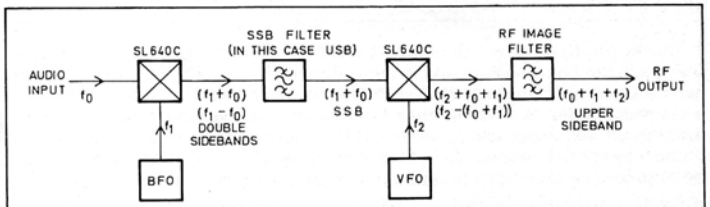


Fig. 47 Basic filter-type SSB transmitter

Fig. 48 shows a more complete filter system. It has an internal amplifier which is controlled by an automatic level control signal which, in most cases, would be derived from the final linear amplifier — either by a threshold detection system or by grid current detection in the output valve.

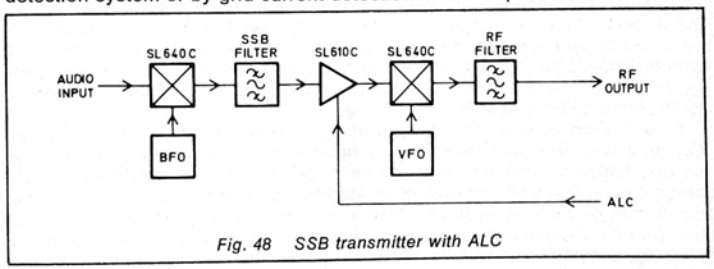


Fig. 48 SSB transmitter with ALC

RF CLIPPING

The envelope of an SSB signal does not resemble the audio producing it. Therefore audio limiting and clipping are not useful techniques for increasing the average to peak power ratio of an SSB transmitter, although audio AGC, derived perhaps from an SL622C, is. Clipping must be applied to the sideband signal itself in the transmitter and the sideband must be filtered to remove intermodulation products. Such a system needs careful initial adjustment but yields good results. A typical system is illustrated in Fig. 49.

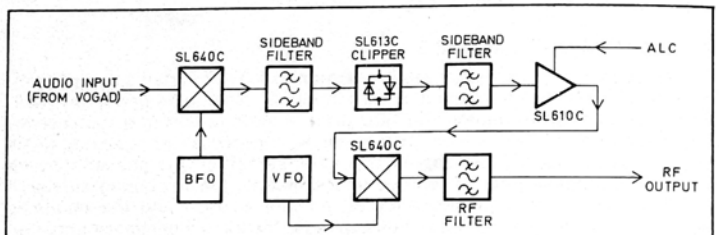


Fig. 49 SSB transmitter with RF clipping

The audio input — which should be controlled by AGC — is converted to SSB as in the basic system and is then clipped by a symmetrical peak clipper, such as an SL613C or a pair of diodes. The signal is then passed through another sideband filter (to remove harmonics and intermodulation products), through an automatic level control (ALC) amplifier and, finally, is converted to the transmitted frequency. The input audio level (or the clipping level) must be adjusted so that the received audio is of adequate quality.

SSB PHASING EXCITERS

A phasing system is shown in Fig. 50. The audio input, which must normally be of limited bandwidth, is phase shifted so that two audio lines of equal amplitude but separated in phase by 90 degrees are obtained. These audio signals are applied to the carrier inputs, and the two outputs are summed. If the audio reference and carrier reference signals are applied to one modulator and carrier reference signals are applied to one modulator and the audio and the audio and carrier quadrature signals to the second, the LSB outputs will be in phase and will add, and the USB outputs will be out of phase and will cancel. Thus, LSB is obtained. Similarly if audio reference and carrier quadrature are applied to one modulator and audio quadrature and carrier reference to the other, USB is obtained.

This method appears attractive in many respects and has the advantages that no expensive filters are used and that the carrier frequency may be varied so that further conversion may not be necessary. It is compatible with the direct conversion SSB receiver illustrated in Fig. 42 and a very simple transceiver can be built using the two systems. The disadvantage is that to keep the second sideband the required 40dB below the desired sideband the phasing, both audio and RF, must be very accurate — in fact within 2 degrees.

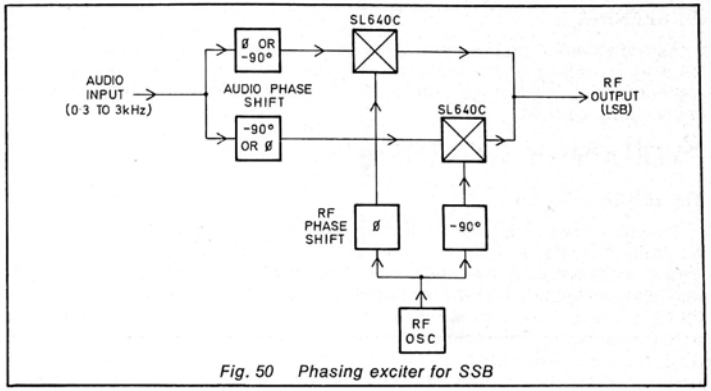


Fig. 50 Phasing exciter for SSB

In addition, the amplitude of the carrier applied to one modulator must be critically adjusted to minimise second sideband generation, and carrier leak must be minimised on both modulators.

Despite the adjustment problems, this method of SSB generation is popular — probably because of the saving of expensive filters.

AMPLITUDE MODULATION

Amplitude modulation can be regarded as DSB with unsuppressed carrier. An SL640C can therefore be used as an amplitude modulator if its carrier leak is increased. If a 15 kilohms resistor is connected between pin 2 of an SL640C and earth (as in Fig. 51) there will be sufficient carrier leak for the output of the SL640C to be AM. A simple method of selecting either AM or DSB can be implemented by switching the resistor in or out of circuit as required. If the filters following the SL640C are also switched, AM, DSB or SSB may be obtained from one SL640C with the same inputs. A multimode transmitter A multimode transmitter can therefore be made with very few components.

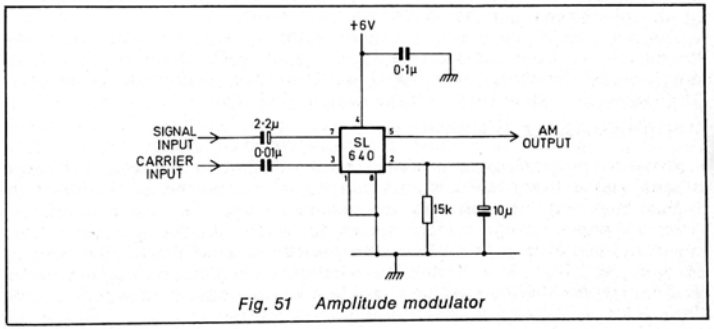


Fig. 51 Amplitude modulator

SCREENING

As transmitters often contain large RF fields, particular attention must be paid to screening and decoupling. In some cases it may be necessary to decouple individual stages. In areas of high field device cans should be individually earthed.

Synthesiser systems

GENERAL

Fig. 52 shows a typical frequency synthesiser. It consists of a voltage controlled oscillator, a variable divider and a phase comparator. The output frequency of the VCO is a function of an applied control voltage. In frequency synthesisers the function is always monotonic and is generally as near linear as possible.

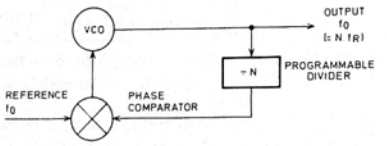


Fig. 52 Basic frequency synthesiser

The output of the phase comparator is a voltage which is proportional to the phase difference between the signals at its two inputs. This output controls the frequency of the VCO so that the phase comparator input from the VCO via the variable divider ($\div$N) remains in phase with the reference input, f_R, so that the frequencies are equal. The VCO frequency is thus maintained at Nf_R, Such a synthesiser will produce a number of frequencies separated by f_R and is the most basic form of phase locked synthesiser. Its stability is directly governed by the stability of the reference input f_R, although it is also related to noise in the phase detector, noise in any DC amplifier between the phase detector and the VCO and the characteristics of the low-pass filter usually placed between the phase comparator and the VCO.

The design of frequency synthesisers using the above principle involves the design of various sub-systems; including the VCO, the phase comparator any low-pass filters in the feedback path, and the programmable dividers. The following deals mainly with the design of dividers.

PROGRAMMABLE DIVISION

A typical programmable divider is shown in Fig. 53. It consists of three stages with division ratios K_1, K_2 and K_3 which may be programmed by inputs P_1, P_2 and P_3 respectively. Each stage divides by K_n except during the first cycle after the program input P_n is loaded when it divides by P, which may have any integral value from 0 to (K-1). Hence the counter illustrated divides by $P_3(K_1K_2) + P_2K_1 + P_1$ and when an output pulse occurs the program inputs are reloaded. The counter will divide by any integer between 1 and $(K_1K_2K_3 - 1)$.

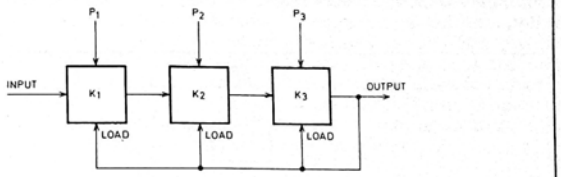


Fig. 53 Typical programmable divider

The commonest programmable dividers are either decades or divide-by-sixteen counters. These are readily available in various logic families, including CMOS and TTL. It is possible to buy quad decades in CMOS in a single package. Using such a package one can program a value of N from about 3 to 9999. The theoretical minimum count of 1 is not possible because of the effects of circuit propagation delays. The use of such counters permits the design of frequency synthesisers which are programmed with decimal thumbwheel switches and use a minimum of components. If a synthesiser is required with less obvious frequencies and steps a custom programmable counter may be made using some custom logic family such as PMOS, NMOS, CMOS or I^2L.

The maximum input frequency of such a programmable counter is limited by the speed of the logic used, and more particularly by the time taken to load the programmed count. Few programmable counters of the type discussed will operate with test frequencies much above 5MHz. The faster types, operating perhaps 25 or 30MHz, use Shottky TTL which consumes considerable power and has a tendency to inject HF and VHF noise into supply lines. The output frequency of the simple synthesiser in Fig. 52 is of course limited to the maximum frequency of the programmable divider.

There are many ways of overcoming this limitation on synthesiser frequency. The VCO output may be mixed with the output of a crystal oscillator and the resulting difference frequency fed to the programmable divider; the VCO output may be multiplied from a low value in the operating range of the programmable divider to the required high output frequency. Alternatively, a fixed ratio divider capable of operating at a high frequency may be interposed between the VCO and the programmable divider. These methods are shown in Figs 54, 54b and 54c respectively.

All the above methods have their problems although all have been used and will doubtless continue to be used in some applications. Method (a) is the most useful technique since it allows narrower channel spacing or higher reference frequencies (hence faster lock times and less loop-generated jitter) than the other two but it has the drawback that since the crystal oscillator and the mixer are within the loop, any crystal oscillator noise or mixer noise appears in the synthesiser output. Nevertheless, this technique has much to recommend it.

The other two techniques are less useful. Frequency multiplication introduces noise and both techniques must either use a very low reference frequency or rather wide channel spacing. What is needed is a programmable divider which operates at the VCO frequency — one can then discard the

techniques described above and synthesise directly at whatever frequency is required.

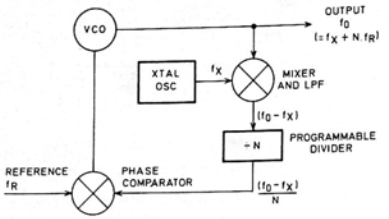


Fig. 54a Mixer synthesiser

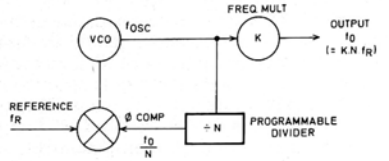


Fig. 54b Synthesiser with ouput multiplication

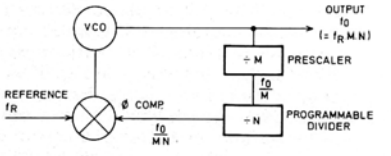


Fig. 54c Synthesiser with prescaler

TWO-MODULUS DIVIDERS

Considerations of speed and power make it impractical to design programmable counters of the type described above, even using ECL, at frequencies much into the VHF band (30 to 300MHz) or above. A different technique exists, however, using two-modulus dividers.

Fig. 55 shows a divider using a two-modulus prescaler. The system is similar to the one shown in Fig. 54c but in this case the prescaler divides either by N or N + I depending on the logic state of the control input. The output of the prescaler feeds two normal programmable counters.

Counters 1 controls the two-modulus prescaler and has division ratio A. Counter 2, which drives the output, has a division ratio M.

In operation the ÷N/N+ I prescaler (Fig. 55) divides by N+I until the count

in programmable counter 1 reaches A and then divides by N until the count in programmable counter 2 reaches M when both counters are reloaded, a pulse passes to output and the cycle restarts. The division ratio of the whole system is A(N+I) + N(M—A), which equals NM+A. There is only one constraint on the system — since the two modulus prescaler does not change modulus until counter 1 reaches A the count in counter 2 (M) must never be less than A. This limits the minimum count the system may reach to A(N+1) where A is the maximum possible value of count in counter 1.

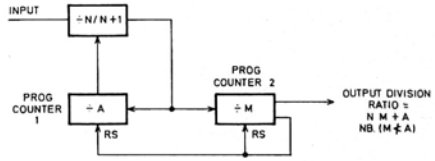


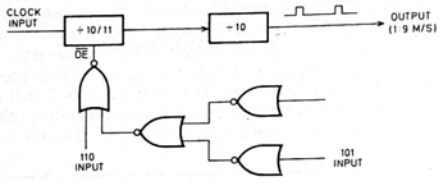
Fig. 55 Divider system with 2-modulus prescaler

The use of this system entirely overcomes the problems of high speed programmable division mentioned above. Plessey Semiconductors make a number of ÷10/11 counters working at frequencies of up to 500MHz and also ÷5/6, ÷6/7 and ÷8/9 counters working up to 400MHz. There is also a pair of circuits intended to allow ÷10/11 counters to be used in ÷40/41 and ÷80/81 counters in 25kHz and 12.5kHz channel VHF synthesisers.

It is not necessary for two-modulus prescalers to divide by N/N+1. The same principles apply to ÷N/N+Q counters where Q is any integer but ÷N/N+1 tends to be most useful.

If the limitation that M must not be less than A is unacceptable the system may be extended to use three or four modulus division. For example if a ÷10/11 prescaler is used in a VHF synthesiser to be programmed in decades the maximum value of A will be 9 and so the minimum frequency will be 99MHz (=A(N+1)). Suppose instead that a ÷100/101/110 counter (which may be made as shown in Fig. 56) is used in the system in Fig. 57. At the start of a cycle the counter divides by 110 until the programmable counter reaches A. This releases the inhibition on programmable counter 2 and the prescaler divides by 101 until counter 2 reaches A_2, at which point the prescaler divides by 100 until counter 3 reaches N and the cycle restarts. The division ratio is therefore $110A_1+101A_2+100(N—A_1—A_2)$ which, by a bit of algebra, is equal to A_2+10A_1+100N.

This system allows a minimum count in the programmable counter 3 of A_1+A_2. Since the system is decimal the maximum value of A_1 and A_2 is 9. The minimum value of N is therefore 18 and if the earlier system is replaced with this system it will work down to 18MHz. A similar, but more complex system involving ÷100/101/111 prescaler allows operation down to 10MHz.



LOGIC

INPUT		COUNT
101	110	
L	L	100
H	L	101
L	H	110
H	H	110

Fig. 56 Basic 100/101/110 prescaler

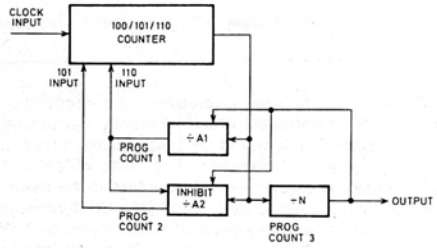


Fig. 57 Divider system with 100/101/110 prescaler

PLESSEY PROGRAMMABLE DIVIDERS

Plessey Semiconductors only manufacture decade or ÷16 programmable counters as custom designs. Programmable dividers for use at 27MHz in Citizens' Band transceivers are, on the other hand, manufactured by Plessey Semiconductors as standard products, and are adaptable for many other applications. Block diagrams of two of these circuits, the SP8921 and SP8922, are shown in Fig. 58.

The M counter of Fig. 58 normally divides by 128. Assume that a ÷N pulse occurs: if R/T1 is high, the ÷N pulse loads 91 into the M counter, so that it divides by 37 (+1 because the load is synchronous) for one cycle; if R/T1 is low, M divides by 128+1 for one cycle. The M counter then reverts to dividing by 128.

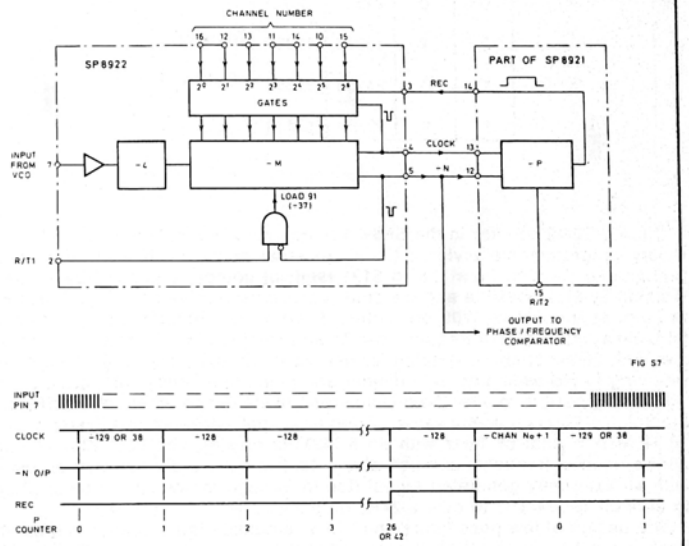


Fig. 58 SP8921 and SP8922 block diagrams

The ÷N pulse also zeros the P counter which programmable to recognise 26(R/T2 high) or 42(R/T2 low). A clock output occurs at the end of each cycle of the M counter and increments the P counter by 1. When P = 26 (or 42) its REC. output goes high for one cycle of M. At the end of that cycle when M has counted 128×25 (or 128×41), plus one cycle of 129 or 38, a clock pulse loads the 'channel select' number into the M counter, which then counts that number +1 (because, once again, the load is synchronous). A ÷N pulse then occurs and a new division sequence begins on the next clock pulse.

The total division ratio, from VCO input to ÷N output is therefore:

$$[25 \text{ (or } 41) \times 128] + [38 \text{ or } 129] + [\text{Chan.no.} + 2] \quad \times 4$$

which, after a little arithmetic, yields division ratios programmable from 12960 to 13832 and from 21152 to 22024 in steps of 4.

These ratios are achieved with combinations of Channel No., R/T1 and R/T2 as shown in Table 3.

R/T1	R/T2	Channel No. 1	Channel No. 127	
0	0	21520	22024	Division Ratios
0	1	13328	13832	
1	0	21156	21660	
1	1	12964	13468	

Table 3

If the ÷26/42 counter in the SP8921 is not used but replaced with 6 bits of binary programmable division (using external chips, such as CMOS) programmable division from 128 to 8191 (still, of course, preceded by a fixed division by 4) is possible and the chips can be used in versatile synthesisers at up to about 35MHz. With prescaling, fixed or variable, such a system can be used at much higher frequencies. As an example Fig. 59 shows a synthesiser with 25kHz channel spacing for use up to 200MHz. The SP8921 is worth retaining for its oscillator, 12^{13} divider and phase/frequency comparator.

It is not possible to alter the division ratio of the divider chain of the SP8921 but 2^{13} (÷8192) is a useful value, giving an output frequency of 1.25kHz with a 10.240MHz crystal or 1kHz with an 8.192MHz crystal. The oscillator should not be used at frequencies much above 12MHz but the divider may be used with an externally generated signal (fed in through the oscillator pins) of up to at least 16.384MHz to give a 2kHz output.

The design of low pass filters and VCOs is outside the scope of this handbook, except to say that the Plessey SP1648 can be used as a VCO in CB synthesisers.

Further information on the design of frequency synthesisers can be found in one of the standard works on the subject such as *Frequency Synthesis* by V.F. Kroupa (Griffin, London) or *Phaselock Techniques* by F.M. Gardner (J. Wiley & Sons).

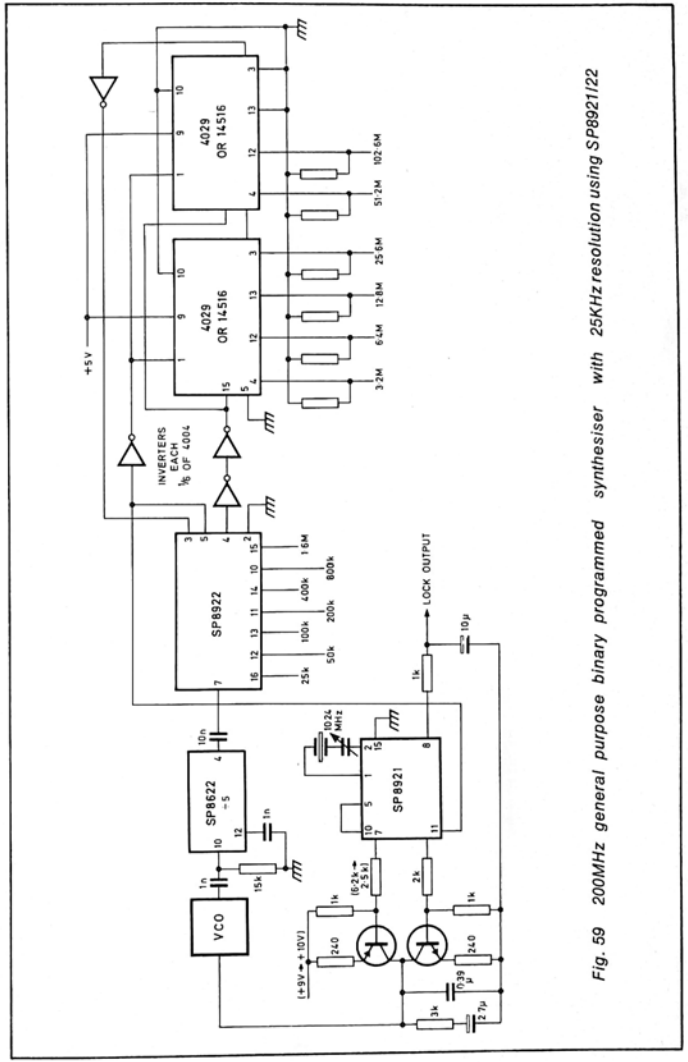


Fig. 59 200MHz general purpose binary programmed synthesiser with 25KHz resolution using SP8921/22

Section 3
Applications

Applications

Sections 1 and 2 of this handbook describe Plessey Semiconductors' range of integrated circuits for Radio Communications and general techniques of using them. This section describes a number of specific applications of these circuits which have been developed at various times in our Applications Laboratory.

These applications cover receivers and transceivers of several types and some frequency synthesisers. Some of these applications have been developed in great detail and are engineered practically to pre-production status, others are merely ideas which have been shown to be practical but have not been taken further.

An AM receiver using SL1600 circuits

This receiver is a single conversion superhet using SL1600 devices with an IF of 455kHz. It was designed for use in 27MHz CB receivers, possibly following another conversion to a first IF of about 10.7MHz. The receiver has a sensitivity of about 1 microvolt and delivers 3 watts to an 8 ohm loudspeaker.

The block diagram of the receiver is shown in Fig. 60. It consists of a normal single conversion superhet with a 455kHz intermediate frequency. An SL1641 double-balanced modulator acts as a mixer and is followed by a ceramic ladder filter with a $\pm$3kHz passband.

The intermediate frequency amplifier consists of three SL1612 amplifiers with a simple interstage ceramic filter between the second and third stages. This amplifier has a gain of over 100dB and AGC is applied to all three stages. It is followed by an SL1623 detector which also provides AGC.

The AGC line may be fed to an external 'S' meter and also goes to an SL748 used in a squelch system. After passing the squelch gate the audio goes to a TBA800 3-watt amplifier.

Fig. 61 is a detailed circuit diagram of the receiver.

THE MIXER

The mixer consists of an SL1641 double-balanced modulator. The SL1641 has a free collector output which is used to drive a 2 kilohm resistive load to provide the correct match to the Murata CFR 455H ceramic filter.

The SL1641 is intended to drive a load with a DC resistance which does not exceed 800 ohms. To prevent saturation of the output transistors of the SL1641, the 2 kilohm resistor must be connected to a +12V supply while the SL1641 itself runs from +6V. Furthermore, it is essential to decouple the supply to the 2 kilohm load most throroughly to prevent IF feedback via the supply line.

This mixer has several advantages — it has a conversion gain of 9dB (which is sufficient to overcome the loss of a CFR 455H filter), a low noise figure, and it requires only 200mV rms of local oscillator injection. It has a signal input impedance of 1 kilohm in parallel with 5pF, which means that it can be driven from a ceramic filter in dual conversion receivers. The local oscillator port also has a high input impedance: 1 kilohm in parallel with 4pF.

The other feature important in a receiver mixer is intermodulation. While the SL1641 cannot compete with hot carrier diode or FET ring mixers, it has considerably better performance than the transistor or FET mixers generally used in Citizens' Band receivers. Its third order intercept point is around +8dBm.

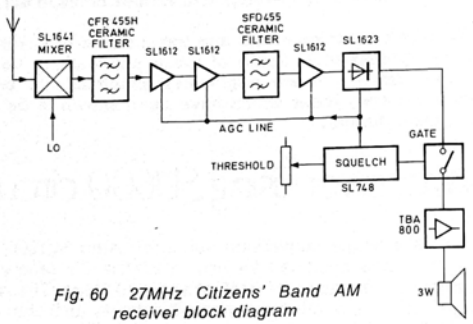


Fig. 60 27MHz Citizens' Band AM receiver block diagram

THE IF AMPLIFIER

The IF amplifier consists of three cascaded SL1612s, giving a maximum gain of over 100dB. Since SL1612 amplifiers are broadband devices, a 100dB untuned strip would have over 20mV of broadband noise at its output, and any local oscillator signal getting through the first filter would be amplified. Extra filtering is therefore necessary, and is provided by a simple SFD 455 between the second and third stages.

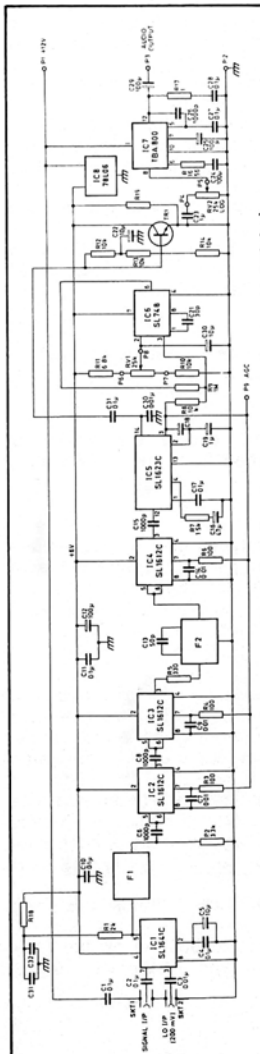
Although the three SL1612s have a maximum gain of over 100dB, the IF strip is stable without any particular precautions — provided that the supply rail is adequately decoupled and the ground layout is adhered to. The receiver may be built on single-sided circuit board without trouble or it may be built on ground-plane double-sided board, in which case both sides of each integrated circuit ground connection must be soldered.

AGC is applied to all three stages. This is not absolutely necessary since two stages will give 140dB gain control range but it is better to have distributed AGC. If AGC is applied to only two stages it should be applied to the first two.

This IF amplifier has excellent performance and uses few discrete components. Although the integrated circuits are more complex than the discrete transistor equivalent, the saving in tuned circuits, discrete components, and adjustment makes the integrated circuit amplifier far superior in both performance and cost.

THE DETECTOR AND SQUELCH

The detector consists of an SL1623. The circuit detects AM and provides carrier-derived AGC which may also be used to drive an 'S' meter. The 'S'



Resistor values are in ohms, capacitor values in microfarads unless otherwise stated.

IC1	SL1641C	R13	10k	C14	0.01	SKT1	Signal input
IC2	SL1612C	R14	10k	C15	1000pF	SKT2	LO input (200mv)
IC3	SL1612C	R15	1k	C16	47 TANT		
IC4	SL1612C	R16	56	C17	0.1	P1	+12V supply
IC5	SL1623C	R17	1	C18	0.1 TANT	P2	Ground
IC6	SL748C	R18	100	C19	1 TANT	P3	Audio output
IC7	TBA800	R19	10k	C20	0.01 TANT		
IC8	78L06	C1	0.1	C21	30pF	P4}	Volume control
R1	2k	C2	0.01	C22	10 TANT	P5}	
R2	3.3k	C3	0.01	C23	1 TANT	P6}	Squelch control
R3	100	C4	0.1	C24	100 TANT	P7}	
R4	100	C5	10 TANT	C25	100 TANT	P8}	
R5	330	C6	1000pF	C26	1000pF	P9	AGC line
R6	100	C7	0.01	C27	0.1	VR1	25k lin squelch control
R7	1.5k	C8	1000pF	C28	0.1	VR2	25k log volume control
R8	10k	C9	0.01	C29	100 TANT	T1	Small signal audio si NPN
R9	1M	C10	0.1	C30	10 TANT	F1	455kHz Murata ladder filter boards
R10	10k	C11	0.1	C31	0.1 TANT		will accept CFS, CFR or CFM types.
R11	6.8k	C12	100 TANT	C32	10 TANT		Recommended is CFR 455H.
R12	10k	C13	56pF			F2	Murata SFD 455D

Fig. 61 27MHz Citizens' Band AM receiver circuit diagram

meter should consist of a voltmeter with a 2V offset reading from 2V (no deflection) to 3.5V (full deflection). It should not draw more than 600 milliamps and should be calibrated linearly.

The AGC is also applied to an SL748 operational amplifier which is used as a squelch circuit. The SL748 is connected as a trigger circuit with a variable threshold so that, as the AGC output rises past the threshold, the squelch output goes high. This high output applies bias to an emitter follower in the audio line which allows the detected audio to pass, via the volume control, to the output stage.

The squelch output may also be used to turn on a lamp to indicate the presence of a signal.

The SL1623 is an AM and SSB detector and has 14 pins. As the SSB facility is not needed it may be replaced by the SL1625 — a version of the SL1623 without the SSB facility and encapsulated in an 8-lead minidip.

THE OUTPUT STAGE

The output stage uses standard 3 watt integrated circuit output stage which will drive an 8 ohm loudspeaker.

POWER SUPPLIES

The mixer and the output stage require a +12V supply, the rest of the circuits a +6V supply. The +6V supply is obtained from the +12V supply with a 78L06 voltage regulator.

LAYOUT

The layout and component placing of the prototypes of this receiver are shown in Figs. 62a and 62b. Other layouts may be used to occupy available space, but two considerations are necessary — the mixer and IF strip should be separated as much as possible (at least 2cm), and the topology of the IF strip layout should be retained to prevent ground loop instability.

PERFORMANCE

The overall performance of this receiver depends on the system in which it is used. Dual conversion systems have good image and spurious performance but single conversion systems have better intermodulation performance. In this performance summary parameters influenced by the external design are therefore ignored.

In the Citizens' Band service at 27MHz the noise figure of a receiver is less important than its strong signal performance. This receiver has a sensitivity of 1 microvolt at the SL1641 input for a 20dB S/N ratio, which is adequate, and a third order intercept point of +8dBm. Its dynamic range is well over 100dB.

On standby the power consumption is about 600mW, although this rises during periods of high audio output.

Receiver passband and adjacent channel rejection depend on the filter used — with a CFR 455H the passband is ±3kHz and adjacent (±10kHz) channel rejection is 65dB.

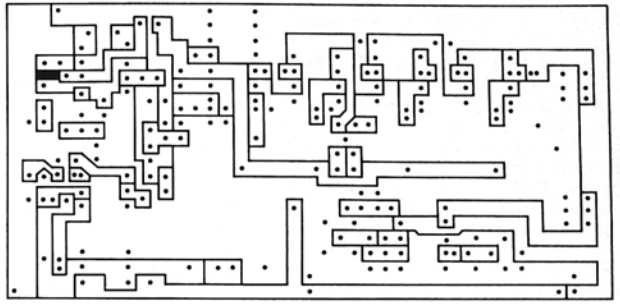


Fig. 62a Printed circuit layout for SL1600C AM Citizens' Band receiver. Scale 1:1

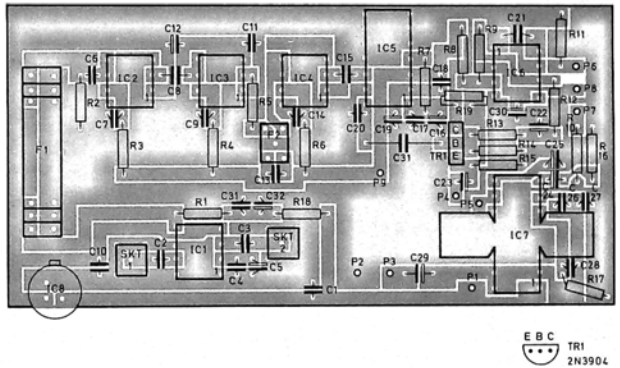


Fig. 62b Component layout for SL1600C AM Citizens' Band receiver. Scale 1:1

Simple SSB transceiver

SL600 VERSION

This transceiver, shown in Fig.63, consists of a single conversion superhet receiver with a 9MHz IF and a very efficient audio-derived AGC system, and a filter type SSB generator, also working at 9MHz. Audio AGC in the modulator path gives constant level output. The transmitter and receiver are arranged so that no signal switching is required between transmit and receive, and the RF components are common to both.

The RF input is direct to an Anzac MD-108 (or similar) hot carrier diode ring mixer. This has 50 ohm ports and is also driven by the local oscillator, at about +7dBm (500mV). The output is connected via a 3: 1 step-up transformer to a 9MHz crystal filter. This filter has the 2.4kHz bandwidth required for SSB and a 90dB stopband. Filters with 60dB stopband can be used, but additional filters may be required at low local oscillator frequencies to keep the local oscillator signal out of the IF amplifier (and the overall receiver performance will, of course, be degraded).

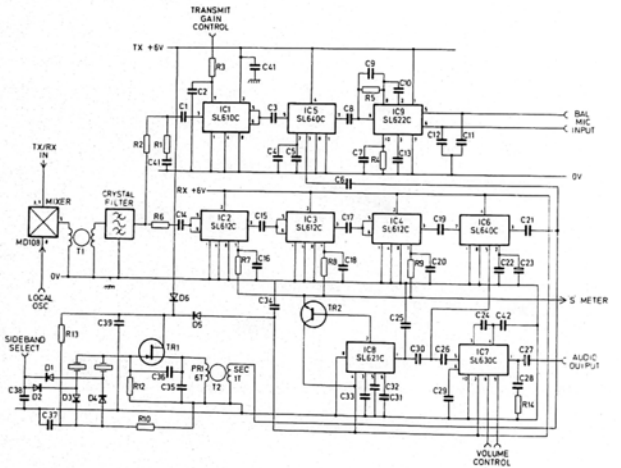


Fig. 63 Simple SSB transceiver circuit diagram

The filter used, an SEI QC1246AX or a KVG XF9-B, has a terminating impedance of 500 ohms, but only within the passband of the filter. At frequencies outside the passband it may be very different, which means that the impedance that the filter presents to the diode ring mixer via the transformer will vary from 50 ohms. Such a mismatch will degrade the cross-modulation and carrier leak performance of the diode ring. However, it was decided on balance, that it was better to tolerate such degradation — which is not excessive — than to complicate the design by incorporating a broadband impedance match (which would probably not be bidirectional and hence would have to be switched between transmit and receive).

The present design allows the same arrangement to operate in opposite directions during receive and transmit without any switching. On the other side of the crystal filter the transmit and receive signal paths diverge but are still not switched.

The Receiver

The incoming RF signal is mixed with the local oscillator in the mixer described above and then passes through an SSB bandwidth 9MHz crystal filter. It is then amplified by three cascaded SL612C IF amplifiers, IC2, 3 and 4. These amplifiers are untuned and since the strip has a maximum gain of 102dB careful attention must be paid both to noise and to stability. The SL612C has a 3dB noise figure which means that the broadband noise at the output of the three-stage strip is about 10mV RMS. This is not sufficient to affect a product detector, which is only concerned with the component within a few kHz of the BFO frequency, but would cause trouble if a diode detector were to be used.

A broadband amplifier with 102dB gain is a likely candidate for stability problems. The three-stage strip used in this receiver is less liable to power supply feedback than most since the SL612C has internal supply decoupling. Nevertheless it must be carefully laid out to minimise earth loops and input/output feedback. The simplest way to do this is to use a double-sided printed circuit board with the components side a continuous ground plane to which all earth connections are made. If this is done the layout on the conductor side of the board is not very critical but if single-sided board is used with the earth conductors on the same side as the other conductors then it does become so. The design of board in Fig. 64 is the most stable layout yet developed for such strips on single-sided board, and it is strongly recommended that it be copied exactly.

There are two other possible causes of instability in this transceiver: inadequate supply switching and inadequate supply decoupling. Since the only on-board transmit/receive switching is by means of power switching it is essential that the transmit supply be not only isolated but earthed during receive, and vice versa. Both supplies should also be well decoupled at RF.

The IF strip has AGC applied to it by an SL621C audio AGC circuit, IC8.AGC is applied via an emitter follower, which has the effect of reducing the AGC range of each SL612C by 0.7V. The overall AGC range could be reduced to less than 90dB were only two SL612Cs to have AGC applied to them. AGC is therefore applied to all three to give 130dB, of which the usable AGC range is about 115dB.

The IF output is applied to an SL640C double-balanced modulator (IC6), used here as a product detector. When AGC is operating, the audio output of

the detector is about 10mV RMS. The audio is fed to IC7, an SL630C audio amplifier which has a voltage gain control. The SL630C can supply up to about 60mW to headphones, to a small loudspeaker or to an external amplifier.

The detected audio also goes to the SL621C audio AGC system (IC8). This has an ideal characteristic for SSB reception. It operates from the receiver audio, not from RF, and it has fast attack and fast decay unless a signal disappears altogether — as in speech pauses — when it does not decay at all for a second and then, if the signal has not reappeared, decays quickly. This enables it to track rising or fading signals but prevents it overloading after each brief speech pause. The circuit also incorporates very fast AGC action to suppress brief noise bursts.

An FET oscillator is used to supply carrier to the product detector and to the double-balanced modulator in the transmitter. The voltage applied to the 'sideband select' terminal determines which crystal is used — upper or lower sideband — but the terminal must not be left unconnected: it must either be connected to +6V or to earth. The oscillator is supplied via diodes from both the transmit and receive lines so that it continues to operate on transmit or receive.

The most basic receiver does not have an 'S' meter but if one is required it may be connected to the emitter of the AGC buffer transistor. It should consist of a moving coil meter connected in series with a resistor such that FSD corresponds to 2.5V and three forward biased silicon diodes. This 'S' Meter circuit has a rather compressed scale for signals more than 40dB above the AGC threshold. If a more linear scale is necessary the more complex system described in the multimode transceiver should be used.

This receiver has a sensitivity of 1.0 microvolts for 10dB S/N. This means that at HF with adequate antennas no RF amplifier is required since atmospheric noise will limit system performance. At higher frequencies, or in systems where small antennas are used, RF gain may be necessary to prevent the performance being gain-limited rather than noise limited. Such amplifiers increase gain but degrade intermodulation performance. In general, without the RF amplifier, the receiver will tolerate about 200mV of adjacent channel signal on the mixer without significant intermodulation. This is, of course, a property of the mixer rather than of the rest of the circuit, although the filter characteristics are also involved.

The Transmitter

The transmitter uses the standard filter method of generating SSB. Audio from the microphone is fed to an SL622C microphone amplifier (IC9), which has AGC giving a constant 100mV output over 60dB of input. The AGC ensures an almost constant output from the transmitter, but can be inconvenient in noisy environments when the transmitter will give full modulation on noise in the absence of a speech input. Such noise modulation is avoided by the addition of a single extra resistor (R5, between pins 8 and 9 of the SL622C) which reduces the dynamic range of the AGC.

The constant-level audio from IC9 is applied to the signal input of an SL640C double-balanced modulator (IC5). The output of the FET carrier oscillator is applied to the carrier input of IC5 and a double sideband suppressed carrier signal appears at its output. Carrier suppression is of the order of 40dB.

This DSB signal is amplified in an SL610C (ICI). The AGC pin of ICI is brought out from the board and may be used either to preset the system gain or as an ALC connection. The amplified DSB from IC1 is then passed through

the crystal filter, which removes one sideband, leaving SSB. The SSB is mixed to the final transmitter frequency in the diode ring mixer and then goes to a linear amplifier which raises it to the transmitter output level. The output from the diode ring is, of course. lower than the input to the filter and is about 100mV or less into 50 ohms.

The output of IC5 and the input of the first SL612C (IC2) are connected to the same point on the filter via resistors. R6 is merely a buffer resistor but R2 and R1 set the impedance which the filter sees in operation. This varies from 480 ohms on transmit to about 530 ohms on receive, but this small variation does not affect filter performance. The loading effects of a turned-off SL612C during transmission and a turned-off SL610C during reception are similarly insignificant.

The transmitter output (at the diode ring) consists of an SSB signal with carrier below — 55dB and opposite sideband below — 60dB, provided that the carrier oscillator is at the correct frequency. The degree of off-channel spurious signals depends on the crystal filter used: 90dB stopband type gives excellent performance but a cheaper one can sometimes cause trouble.

The Transceiver

The transceiver board needs few extra sub-systems to make a complete transceiver. They are: a power supply, microphone, volume control and loudspeaker and also a filter, local oscillator and linear amplifier. These are connected as shown in Fig. 65.

Much of the performance of the final system will depend upon the standard of design of the local oscillator, pre-selector, RF amplifier (if used) and linear amplifier, but the performance of the transceiver board itself is excellent. The Anzac MD-108 mixer used is capable of the required performance between 10kHz and 500MHz. If other diode rings were used the transceiver might be used over an even wider range. Its power consumption is about 400mW on either transmit or receive.

The most attractive feature of this transceiver, despite its high performance, is its simplicity. It uses only 80 components and contains no tuned circuits or other components requiring adjustment. It was designed for two purposes: (a) to demonstrate the usefulness and versatility of the SL600 Series in SSB applications and (b) as a ready-engineered SSB transceiver suitable for those inexperienced in SSB design. It is capable of giving good performance but can be constructed and commissioned by relatively inexperienced personnel.

Physical Construction

The board and component layouts are shown in Fig. 64. The board is single-sided and there are two jumper links on it carrying power supplies. As mentioned above the layout on a single-sided board carrying such a high gain broadband IF strip is critical and it should not be changed. All passive component leads should be as short as possible and integrated circuits should not be mounted more than 6mm above the board.

The two transformers T1 and T2 are both wound on small toroids of high frequency ferrite. The exact size and material are not important but the material must be low loss up to at least 45MHz and it is essential that it has a linear B/H characteristic, otherwise it will cause intermodulation at the receiver

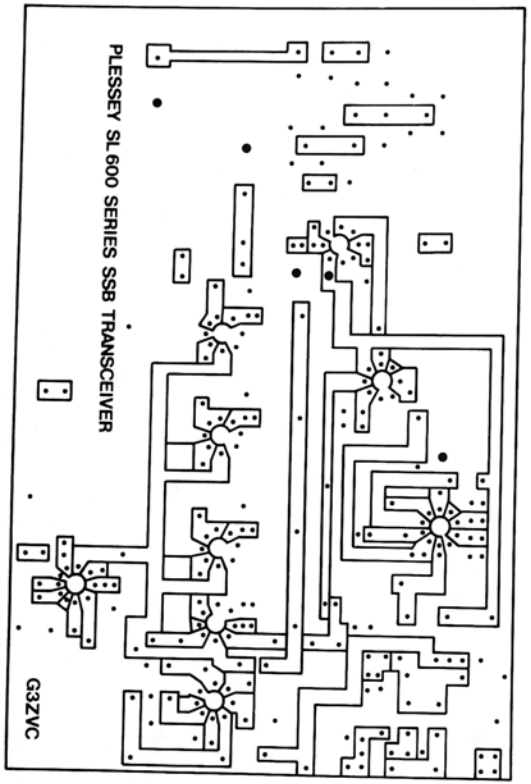


Fig. 64a Copper side of PCB for simple SSB transceiver

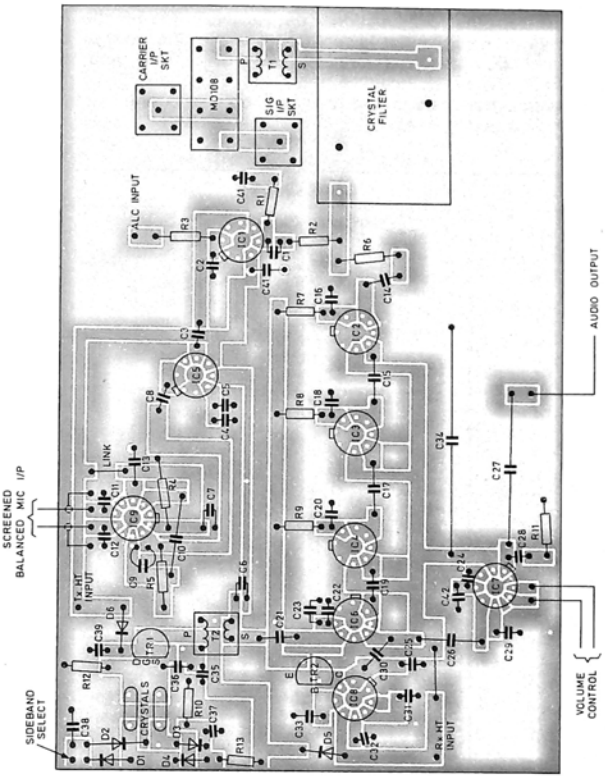


Fig. 64b PCB for simple SSB transceiver

input. T2 is a simple transformer with a six-turn primary and a single turn secondary but T1 is more complex. T1 is made from four 5cm lengths of 26 SWG (0.46mm dia.) enamelled copper wire twisted together. The length of twist is used to wind two turns on the toroid and the ends are separated. Three lengths are then connected in series in the same sense to form the filter winding and the last length is used as the diode ring winding.

There are few other constructional details that need mentioning, but if a receiver without a transmitter is required one may be built by omitting the three transmitting integrated circuits (SL610C, SL622C and the SL640C) between them), R1 to R5 inclusive and C1 to C13 and C40. To preserve the filter impedance match a 500 ohm resistor should be connected from the filter side of R6 to earth.

Component	Value	Rating	Type
R1	100	1/8 W	Hi-Stab.
R2	430	1/8 W	Hi-Stab.
R3	100	1/8 W	Hi-Stab.
R4	680K	1/8 W	Hi-Stab.
R5	1K	1/8 W	Hi-Stab.
R6	50	1/8 W	Hi-Stab.
R7-R9	100	1/8 W	Hi-Stab.
R10	330	1/8 W	Hi-Stab.
R11	10	1/8 W	Hi-Stab.
R12	100K	1/8 W	Hi-Stab.
R13	330	1/8 W	Hi-Stab.
D1-D6			1N4148 } Or similar
TR1			2N3819 } devices
TR2			2N706 }
T1, T2	See text.		
Mixer	Anzac MD-108		
Crystals	9.0015 MHz & 8.9985 MHz		Parallel (30p) resonant
IC1	SL610C		
IC2-IC4	SL612C		
IC5-IC6	SL640C		
IC7	SL630C		
IC8	SL621C		
IC9	SL622C		
C1-C4	1nF	50V	Weecon (Min Ceramic)
C5	10µF	6.3V	Min. Tantalum
C6	100pF	50	Ceramic
C7	47µF	6.3V	Min. Tantalum
C8	10µF	6.3V	Min. Tantalum
C9	4.7nF	50V	Weecon
C10	2µF	6.3V	Min. Tantalum
C11-C12	1nF	50V	Weecon
C13	100nF	50V	Weecon
C14-C15	100pF	50V	Ceramic
C16	4.7nF	50V	Weecon

Table 4 Components list for the Simple SSB Transceiver (Fig. 63)

Component	Value	Rating	Type
C17	100pF	50V	Ceramic
C18	4.7nF	50V	Weecon
C19	100pF	50V	Ceramic
C20	4.7nF	50V	Weecon
C21	100pF	50V	Ceramic
C22	1nF	50V	Weecon
C23	10µF	6.3V	Min. Tantalum
C24	4.7nF	50V	Weecon
C25	100nF	50V	Weecon
C26	10µF	6.3V	Min. Tantalum
C27	100µF	6.3V	Min. Tantalum
C28	10nF	50V	Weecon
C29	1nF	50V	Weecon
C30	1µF	6.3V	Min. Tantalum
C31	100µF	6.3V	Min. Tantalum
C32	47µF	6.3V	Min. Tantalum
C33	100µF	6.3V	Min. Tantalum
C34	400µF	16V	Min. Al. Elect.
C35-C36	68pF	50V	Ceramic
C37-C38	10nF	50V	Weecon
C39-C41	100nF	50V	Weecon
C42	100pF	50V	Ceramic

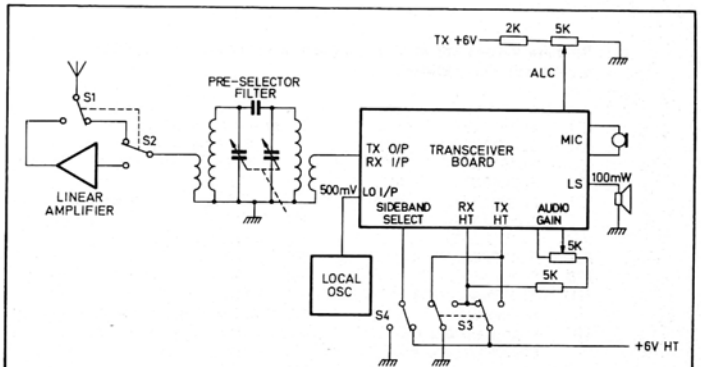


Fig. 65 Block diagram of complete SSB transceiver

SL1600 VERSION OF THE SSB TRANSCEIVER

Figs. 66 and 67 show the circuit diagram and board layout respectively of a version of the SSB transceiver which has been designed to use the SL1600 devices. In addition to the use of the SL1600 series circuits a single PNP transistor is used in place of the SL610 in the transmitter and has only one BFO crystal on the board.

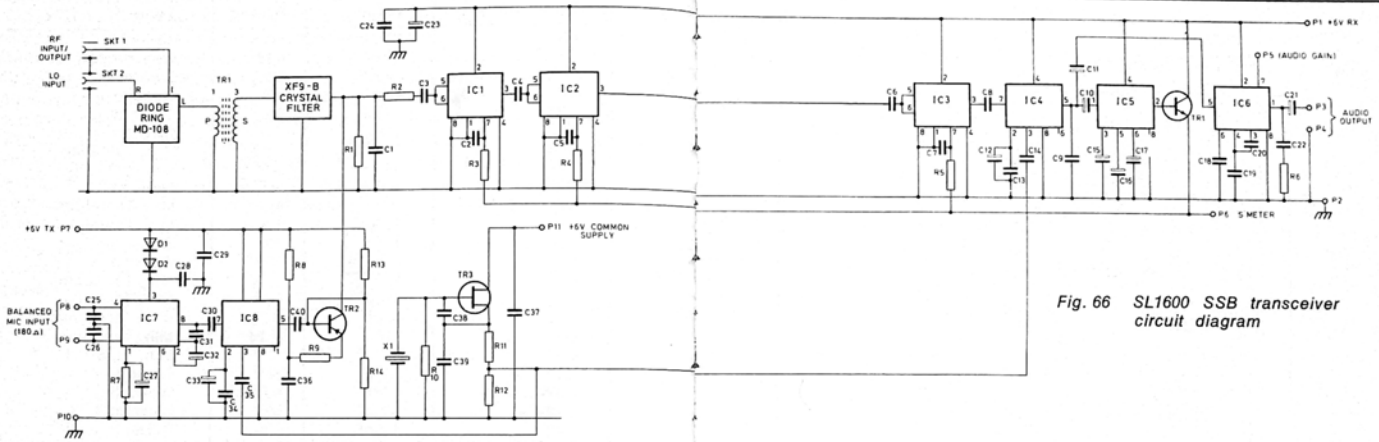


Fig. 66 SL1600 SSB transceiver circuit diagram

Resistor values are in ohms, capacitor values in microfarads unless otherwise stated.

IC1	SL1612C
IC2	SL1612C
IC3	SL1612C
IC4	SL1640C
IC5	SL1621C
IC6	SL1630C
IC7	SL1622C
IC8	SL1640C
TR1	Si NPN – 2N706, BC108 etc.
TR2	High frequency Si PND – 2N3906 etc.
TR3	High frequency N-channel FET – 2N3819, BF244B etc.
D1 D2	Almost any small Si diode – 1N914 etc.
Diode ring – ANZAC MD-108	

Filter – KVG Xf9-B	
X1	30pF parallel resonant 8998 5kHz in HC18 or HC25
T1	P 2 turns 2 hole S 5 turns ferrite bead
R1	470
R2	47
R3	120
R4	120
R5	120
R6	10
R7	470k
R8	100
R9	100
R10	100k
R11	1k
R12	Select to give 200mV rms at pin 4 of IC4
R13	2.7k
R14	8.2k

P1	16V receive supply
P2	Ground
P3	Audio output
P4	Audio ground
P5	Audio gain control
P6	'S' meter (if used)
P7	+6V transmit supply
P8, P9	Balanced microphone input (180 ohms)
P10	Ground
P11	+6V common supply

All resistors 5 per cent $\frac{1}{4}$W

All capacitors miniature ceramic except ones marked TANT which are bead tantalum.

C1	22pF	C31	5000pF
C2	0.01	C32	2 TANT
C3	1000pF	C33	10 TANT
C4	1000pF	C34	0.1
C5	0.01	C35	1000pF
C6	1000pF	C36	0.1
C7	0.01	C37	0.1
C8	1000pF	C38	56pF
C9	0.1	C39	56pF
C10	1 TANT	C40	0.1
C11	1 TANT		
C12	10 TANT		
C13	0.1		
C14	1000pF		
C15	100 TANT		
C16	47 TANT		
C17	100 TANT		
C18	1000pF		
C19	100pF		
C20	5000pF		
C21	100 TANT		
C22	0.01pF		
C23	100 TANT		
C24	0.1pF		
C25	1000pF		
C26	1000pF		
C27	47 TANT		
C28	0.1		
C29	0.1pF		
C30	1 TANT		

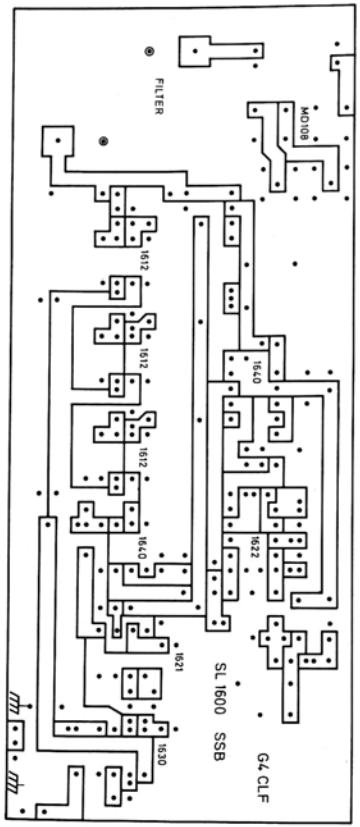
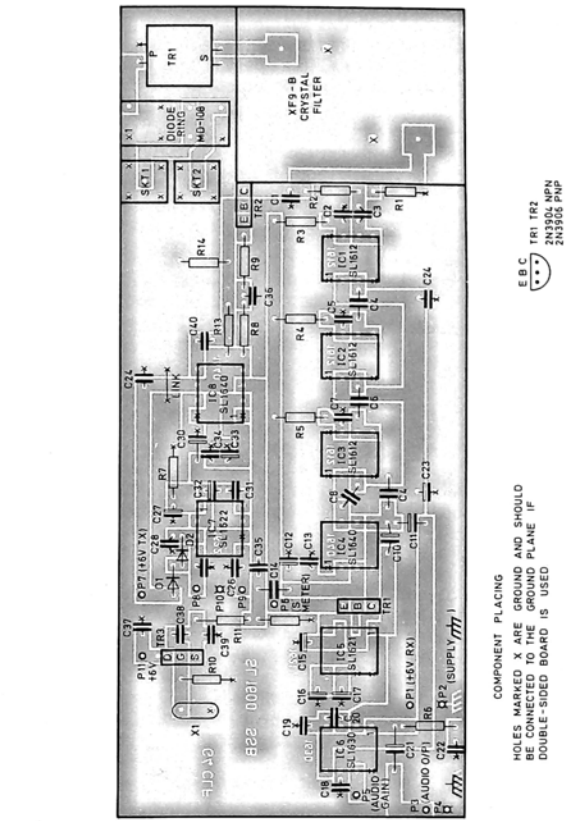


Fig. 67a SL1600 SSB transceiver printed circuit layout. Scale 2:1



Like the simple SSB transceiver this multimode transceiver consists of a single printed circuit board and requires the addition of a local oscillator, pre-selector, power amplifier, microphone, loudspeaker and volume control, as well as power supplies and possibly an RF amplifier, to make a complete transceiver.

The board, the block diagram of which is shown in Fig. 68, contains nearly all the signal processing of the transceiver, including a noise blanker, VOX, dual time constant AGC, an 'S' meter/squelch control and RF compression during transmission. Since most sub-systems work independently the board may be built without such refinements and used — either temporarily as a stage in construction and evaluation, or permanently if particular functions are not required. Thus the board may be used to build many different receivers or transceivers.

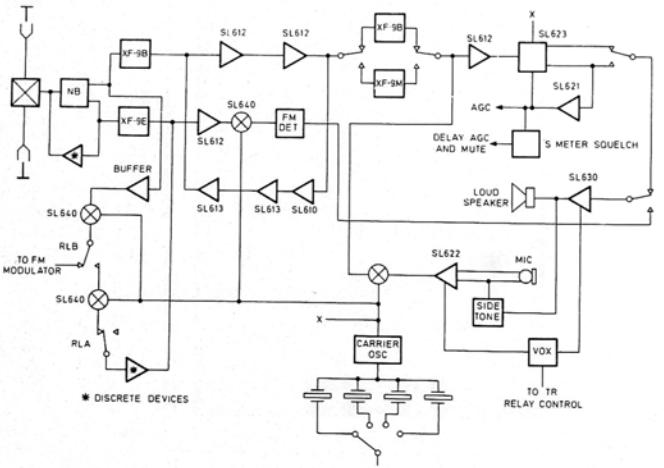


Fig. 68 Multimode transceiver block diagram

RECEIVER DESIGN CONSIDERATIONS

The major problem of receiver design is that of strong signal handling during weak signal reception. There is no single cure for it but designs of high performance receivers usually have as little RF gain as possible, followed by a mixer with good strong signal performance followed at once by a crystal filter. The crystal filter removes the majority of unwanted signals and the rest of the receiver is unlikely to be troubled by them.

The crystal filters do not follow the mixer directly in this receiver, for two reasons: first, to improve the impedance match between the mixer and the filter, and secondly to permit the use of a noise blanker to suppress impulse interference.

A suitable mixer for high performance receivers must have low noise, as little conversion loss as possible, and be able to handle strong unwanted signals without intermodulation. In this transceiver (as a reasonable compromise between cost and performance) a hot carrier diode ring mixer, the MD-108 has again been chosen. Such ring mixers perform best when they are terminated in 50 ohm resistive loads at all ports, but the input impedance of crystal filters, besides being generally higher than 50 ohms, is reactive at frequencies away from the filter passband.

In the Simple SSB Transceiver a transformer matching system was used between the mixer and the filter and the reactive mismatch was ignored. In this system a buffer amplifier, which is in fact also part of the noise blanker, is used to terminate both the mixer and the filter correctly.

A major reason for the failure of receivers to produce weak AM and SSB signals is man-made noise, typically ignition interference, at the antenna. This noise is frequently in the form of very narrow pulses of very high amplitude which can cause the crystal filter to ring at its resonant frequency. Once the filter has been thus stimulated it will stretch the pulse so that it cannot be distinguished from the wanted signal, which it swamps. Only by stopping the ignition pulse before it reaches the filter can this interference be suppressed. The noise blanker must therefore be somewhere in the receiver before the crystal filter and the best place is between the mixer and the filter.

After the crystal filters the receiver design is quite conventional. There are two filters, each feeding its own IF strip. One has a 12kHz passband and feeds the FM IF system, which is a double conversion system with a 455kHz second IF and a quadrature detector. This receiver was designed before the introduction of the SL665, which would allow the use of a single 9MHz IF.

The other filter has a 2.4kHz passband and its output goes to the CW/SBB/AM IF strip. This strip has a broadband gain of about 70dB followed by another crystal filter, which is of 2.4kHz bandwidth for AM and SSB and 500Hz for CW. There is then another IF amplifier stage followed by two detectors. For SSB and CW there is a product detector and for AM there is an envelope detector.

On AM the envelope detector provides carrier AGC to the system but on CW and SSB an audio derived AGC system is used. Squelch and 'S' meter signals are derived from the AGC line.

The decision to use a 2.4kHz filter for AM, removing one sideband, was taken on cost grounds, as was the decision to use only one 500Hz CW filter halfway down the IF strip, whereas two such filters, one at the input to the strip, would certainly improve strong signal rejection in the CW mode. Ideally

there should be four filters at the input (with bandwidths of 12, 6, 2.4 and 0.5kHz respectively for NBFM, AM SSB and CW) and a further three filters halfway down the AM/SBB/CW IF strip to reduce IF noise to a minimum. This would entail an extra three expensive crystal filters compared with the present system — for only a marginal increase in system performance.

The use of two filters halfway down the IF strip is well justified, however. The CW filter in this position removes both unwanted CW signals in the 2.4 kHz passband and also much of the broadband noise which can cause difficulty in copying very weak signals. The 2.4kHz filter is essential to remove the broadband noise between 100kHz and 30MHz generated by the first two IF stages which, if allowed into the AM diode detector, would greatly degrade its performance.

The improvement due to this filter on the SSB product detector is much less, since product detectors produce supersonic outputs from broadband noise and these can be filtered without loss of wanted signal. There is nevertheless a 3dB improvement in S/N ratio in systems where IF noise is the limiting factor on system performance.

TRANSMITTER DESIGN CONSIDERATIONS

The transmitter has to generate all the modes that the receiver has to receive. This is not particularly difficult, but several complexities have been introduced to minimise spurious outputs and broadband noise while making the transmitter as effective as possible.

The modulation envelope of SSB does not resemble the audio producing it and normal audio speech processing techniques do not greatly improve the S/N ratio at the receiver. RF clipping, however, reduces the peak/mean power ratio of the signal and hence improves its mean power and readability.

It is also convenient to use the RF clipper for NBFM and AM, these signals being demodulated from clipped SSB back to audio and the audio signal applied to the NBFM or AM modulators. This technique gives up to 12dB apparent signal to noise ratio improvement and the resulting received audio, while obviously 'processed', is not unpleasant.

The audio input to the transmitter passes through an audio preamplifier with AGC to ensure a roughly constant modulation signal regardless of microphone or audio level. It is converted to DSB in a double-balanced modulator and filtered to SSB which is then applied to a limiting amplifier which removes all amplitude variations. This clipped signal is, of course, rich in both harmonics and intermodulation products and must be filtered in a 2.4kHz bandwidth filter to remove them. The quality of this filter determines the spectral purity of the resulting clipped SSB and is more important than the first filter producing the sideband.

The 2.4kHz bandwidth filter reintroduces amplitude variations into the signal which must be amplified by a linear amplifier. The signal is then either further amplified and mixed to the final transmitter frequency or demodulated to yield processed audio which can be applied to the AM or FM modulators.

The FM system uses this audio to modulate the external VFO while the transceiver board supplies a steady 9MHz output to the transmitter mixer. The AM modulator – which also supplies this unmodulated carrier during FM transmission – consists of a double-balanced modulator with deliberate carrier leak. All transmitted signals pass through a 12kHz filter as they leave the board – this costs nothing since the filter is already present in the FM receiver,

and removes any broadband noise which the buffer amplifiers may have introduced.

The CW transmitter uses the complete SSB system except that a keyed tone is used as the audio input and the 500Hz filter is used instead of the 2.4kHz filter in the SSB generator. This allows only a single frequency to go to the RF clipper, rather than the several frequencies caused by harmonics from the tone generator, which would result from the use of the 2.4kHz filter.

Like the simple SSB transceiver the majority of the transmit/receive switching is performed by switching power supplies and not signal lines. The power switching itself, however, is performed by a relay which can be driven either from a transmit/receive switch or by the VOX system. Mode switching, however, is performed by relays, so that when the transmitter and receiver are in different modes some relays change state between transmission and reception.

TRANSCEIVER SYSTEMS

To use the transceiver board it is built into a system very similar to that used for the Simple SSB Transceiver illustrated in Fig. 65. A small difference is that if FM transmission is required provision must be made for the processed audio from the board to modulate the VFO. Otherwise the two systems are identical – except that rather more power supplies and function switching are required with the multimode transceiver.

Sub-systems may be omitted if a simple transceiver, or just a receiver, is required. Similarly, the board may be built and operated as an SSB receiver, then expanded to an SSB transceiver without RF clipping, then RF clipping added, etc., as required.

CIRCUIT DETAILS

The circuit diagram of the complete transceiver board is shown in Fig. 69. The whole circuit will be described but where sub-systems are built entirely of SL600 devices conventionally used no explanation of circuit configuration will be given. If this is required the reader is referred to Section 1.

The sub-systems into which the board has been divided are described below.

The Mixer

The Anzac MD-108 mixer was chosen for its performance coupled with its low price, but any hot carrier diode ring modulator with 50 ohm ports and adequate strong signal performance (the MD-108 will handle over 200mV RMS adjacent channel signal) combined with low noise and under 7dB conversion loss could be used euqally well. The MD-108 has two ports with 5–500MHz bandwidth and one with DC to 500MHz bandwidth. If the transceiver is used with signals or VFO of under 5MHz it is important to ensure that this signal is applied to the correct port.

It might be thought that the receiver performance on strong signals would be improved by using a better diode ring, able to handle larger signals. This is not in fact so: if the mixer is improved the noise blanker and filter become the limiting factors in the strong signal performance. A mixer with better high or low frequency performance may, however, be substituted if required.

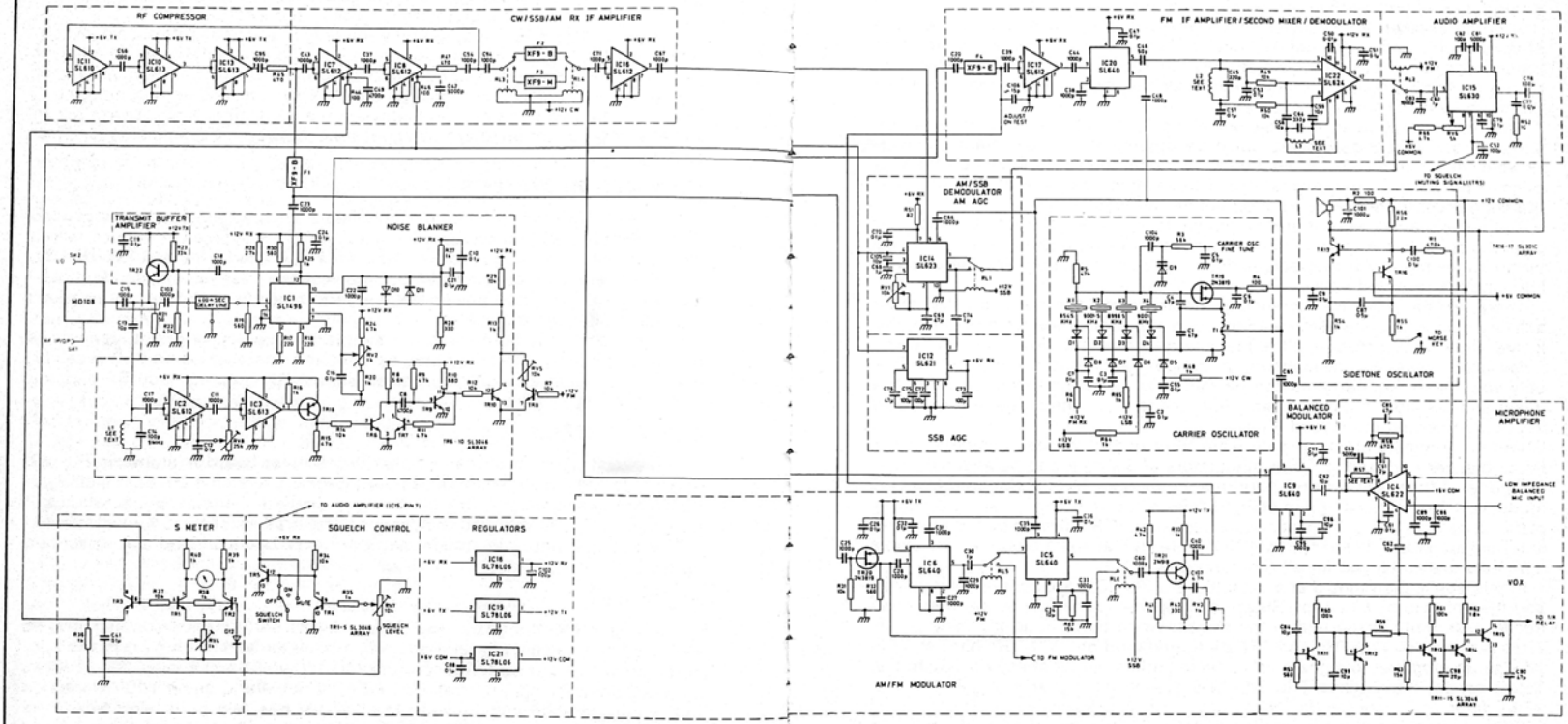


Fig. 69 Multimode transceiver circuit diagram

The Noise Blanker

Probably as much work went into the development of this noise blanker as into the rest of the receiver. It has excellent performance and causes very little degradation of the receiver strong signal characteristics.

A noise blanker is a receiver which receives noise pulses, amplifies and shapes them, and uses them to turn off the main receiver while noise is present. As noise is not evenly distributed throughout the frequency spectrum the noise blanker receiver should be operated in the same frequency band as the main receiver.

This in turn suggests that the noise receiver and the main receiver be common and that the blanking pulse be applied late in the main receiver. However if a noise pulse is applied to a crystal filter it is stretched from its original length of a few microseconds to as much as several milliseconds. Blanking must therefore be applied before the crystal filters.

The noise blanker must therefore stop a noise pulse before it can reach the crystal filter from the mixer. Furthermore if a blanking pulse has sharp (large dV/dt) edges these will themselves act as noise pulses, negating the effect of blanking the received noise.

There are therefore two conflicting requirements: the noise blanker must act very quickly to prevent the leading edge of a noise spike from reaching the crystal filter, and it must apply a blanking pulse with a slow rise time to the noise gate to prevent the blanking pulse from acting as a noise pulse. The only way these requirements can be met is to delay the signal between the mixer and the filter in a linear delay line and to place the noise gate between the delay line and the crystal filter.

Various forms of blanking gate were tried during the development of the noise blanker – including diode modulators and single and balanced FETs – but none of them gave better performance than an SL1496 double-balanced modulator. The circuit diagram of an SL1496 is shown in Fig. 70 and a diagram of the noise gate in Fig. 71. Transistors designated TR followed by a lower case letter subscript are those internal to the SL1496. Transistor designations using numerals are employed for all other devices.

In this application pins 5 and 14 of the SL1496 (IC1) are connected together and the emitters of TRa and TRb are thus open-circuited. They are then connected externally to the rest of the circuit. When there is no blanking pulse TR10 is turned off and TRc and TRf are turned hard on. With TRc hard on TRa acts as an amplifier to signals on its base and its output goes, via TRc to the XF9-B crystal filter. Since TRd and TRe are off no signal is applied to the XF9-E filter.

When a blanking pulse is applied to TR10 it is turned on and TRc and TRf turn off (slowly because of the resistor in TR10 collector and the 1 nF capacitor between inputs 8 and 10 of the SL1496) and TRd and TRe turn on. The signal path is now to F4 and the F1 is isolated – noise cannot pass to the CW/SSB/AM IF strip.

The noise blanker is not effective during FM reception and is not used. Instead TR8 is turned on and this balances the modulator so that TRc, TRd, TRe and TRf are turned on and signals go to both IF strips. This is necessary because the squelch is derived from the CW/SSB/AM strip in all modes, including FM.

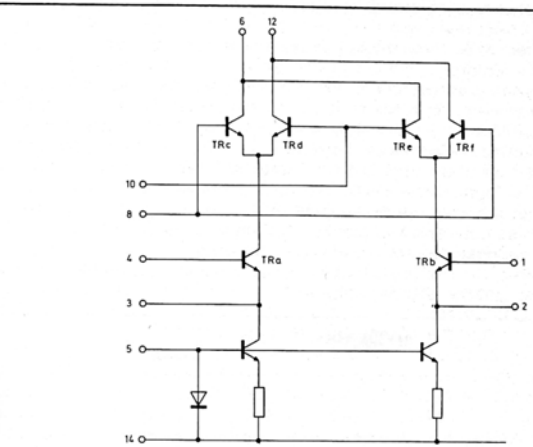


Fig. 70 SL1496C circuit diagram

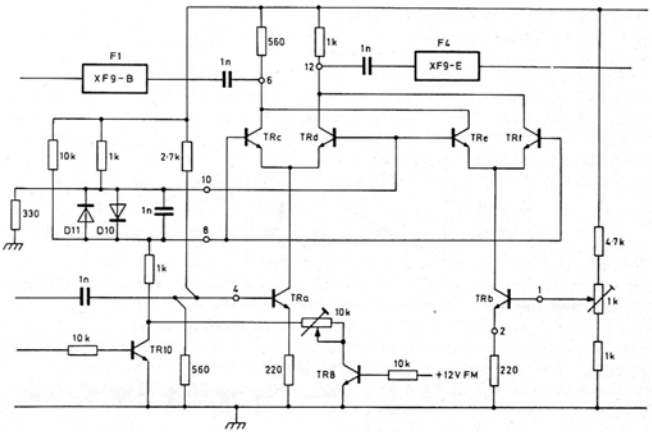


Fig. 71 The noise gate

The diodes between pins 8 and 10 of the SL1496 ensure that the switching drive is at the correct level and the preset current source TR8 keeps the DC current in the filter loads constant as the system switches from the unblanked to the blanked condition.

The whole system is shown in Fig. 72. The noise receiver has its input via a tuned circuit to prevent local oscillator leak from the mixer triggering the system. The noise IF amplifier consists of an SL612C (IC2) and an SL613C (IC3) which acts as a detector. Gain control is applied to IC2 to set the blanking level.

Pulse outputs from the detector in IC3 are buffered by a PNP transistor TR18 to a simple monostable (TR6, TR7 and TR9) with a 10 microsecond pulse. This pulse operates the noise gate. A 400 ns delay line between the mixer and the noise gate ensures that the system is blanked before the pulse that triggers the monostable arrives at the noise gate.

Lastly, a feature of the system is that it acts as a matching amplifier between the 50 ohm mixer and the 500 ohm filters.

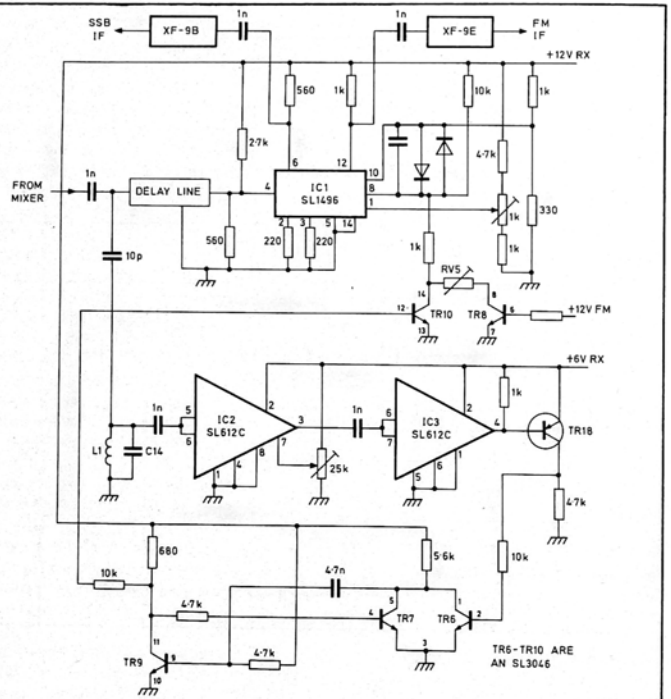


Fig. 72 The noise blanker

The AGC 'S' Meter and Squelch Circuit

As mentioned above the SL623C (IC14) operates as a carrier AGC system during AM reception. It also operates in the same mode during FM reception but does not apply AGC to the FM IF, the AGC line being used only for squelch and to drive the 'S' meter. When the carrier oscillator is turned on, the product detector in IC14 operates and a signal is applied to an SL621C (IC12) connected to its output. The SL621C is more sensitive than the SL623C and so it takes over as AGC source to provide an audio derived AGC system for CW and SSB reception. Since the output impedance of both the SL621C and the SL623C AGC systems are high when they have no input they are both connected to the AGC line and do not load each other.

If fast AGC is required during tuning in the SSB and CW modes, the IC12 may be turned off and control restored to the IC14. This will result in higher outputs but faster decay when tuning from a strong signal. Some professional receivers using SL621C circuits have facilities for dumping AGC from the timing capacitors but it was felt unnecessary to this design.

The AGC line from these two devices drives the second SL612C (IC8) in the CW/SSB/AM IF strip directly and also goes to the squelch and 'S' meter circuitry shown in Fig. 73. TR3 acts as a buffer to drive the squelch circuitry, and also as a diode drop (0.7V) to delay the AGC to IC7. The output of TR3 is filtered by 1 kilohm and 100 nF and applied to a potentiometer ('Squelch Level') and thence to the base of TR4, which acts as an inverter. The inverter output drives TR5 which mutes the SL630C audio amplifier (IC15), by connecting pin 7 of IC15 to earth. A three-position switch which earths either TR4 collector (to disable the Squelch) or TR5 collector (to mute the receiver) is included. Its centre position neither mutes the receiver nor disables the squelch. If a mute position is not required, a single pole on/off switch may be used.

As the AGC characteristic of SL600s is somewhat non-linear, a simple voltmeter on the AGC line does not make a good 'S' meter since it tends to be too sensitive to signal changes near the AGC threshold and not sensitivie enough to large signals. The long-tailed pair TR1 and TR2 with the diode D12 form a compensating circuit. All five transistors in this block of circuitry are on a single chip, the SL3046, in a 14-lead DIL package. This saves board space and gives a good match between TR1 and TR2.

The FM IF Strip and Detector

Double conversion is used in the FM receiver because of the difficulty of providing adequate 'Q' at 9MHz for an NBFM quadrature detector. The 9MHz output from the 12kHz-wide XF9-E filter F4 is amplified by an SL612C (IC17) and is then mixed to 455kHz in an SL640C (IC20). A single tuned circuit is used to remove the image and the signal is then passed to an SL624C working as a limiting amplifier/quadrature detector. This receiver was developed before the SL665 became available – otherwise a single 9MHz filter would have been used and the SL624C replaced by an SL665C.

The CW SSB AM IF Strip

The IF strip is quite conventional. The output of the XF9-B 2.4kHz filter F1 is applied to two cascaded SL612C amplifiers. The output of the second SL612C (IC8) goes either to a 2.4kHz XF9-A or to a 500Hz XF9-M filter, (F3), depending

on whether the receiver is in SSB/AM or in CW mode. The filters are switched by two small relays. After the filter there is another SL612C (IC12) and an SL623C detector (IC14). Without a carrier oscillator IC14 acts as an envelope detector for AM and generates carrier-derived AGC in this mode. When the carrier oscillator is applied IC14 acts as a product detector for SSB and CW and an SL621C (IC12) at the product detector output takes over the AGC. The audio output line must be switched between the two detectors.

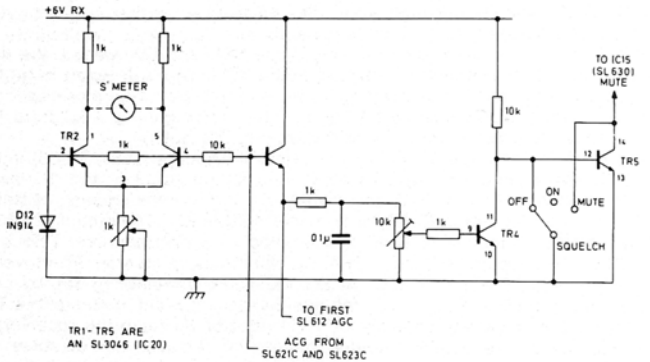


Fig. 73a AGC "S" meter and squelch circuit

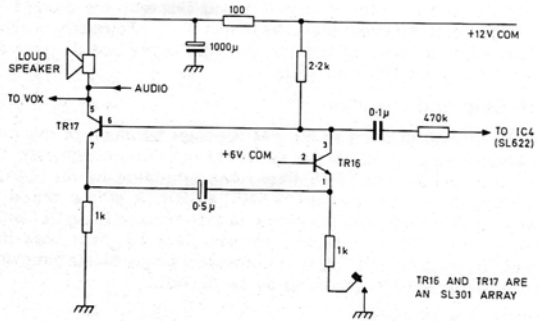


Fig. 73b Sidetone oscillator

The Carrier Oscillator

The carrier oscillator has four different frequencies: 8545kHz for the second mixer in the FM IF system, 8998.5kHz for USB, 9001.5KHz for LSB and 9001 kHz for CW. The circuit is a conventional FET Colpitts oscillator (TR19) and uses diode switching to select one of four crystals.

The output of the oscillator is about 1 volt RMS and is therefore reduced in a potentiometer to the 200mV RMS required by SL640Cs. This potentiometer acts as a virtually constant load to the oscillator and an output buffer is not required.

If the crystals used do not oscillate at their nominal frequency, either the two 47pF capacitors between gate and source and source and ground may be changed in value while remaining equal. Alternatively, where only one or two crystals need trimming, provision is made for crystal trimming by a varicap and a potentiometer for each sideband crystal.

The Audio Amplifier and Sidetone Oscillator

The SL630C audio amplifier (IC15) is driven from a +12V line. It is capable of providing up to 200mW to a small loudspeaker but if a greater output is necessary an additional audio amplifier should be provided. The output of the SL630C is also applied to the VOX circuitry, TR11 to TR15. Gain is controlled by a voltage applied to pin 8 of IC15.

Since the output impedance of the SL630C is quite high when it is turned off, and likewise that of the sidetone oscillator, the loudspeaker is connected directly to both. The sidetone oscillator shown in Fig. 73, is an emitter-coupled multivibrator keyed in the emitter of TR16. A signal is taken from the collector of TR17 and applied to the transmitter audio input.

The sidetone frequency is 1kHz and the system relies on the CW filter to produce a single tone output from the transmitter. If the 500Hz CW filter is omitted the frequency should be raised to about 1750Hz to place the second harmonic well down the SSB filter characteristic. In amateur transceivers an accurate 1750Hz may have an additional use as a repeater access tone.

The Microphone Amplifier and SSB Generator

The audio from the microphone (or the CW from the sidetone oscillator) is amplified by an SL622C (IC4). The SL622C contains its own AGC circuitry with fast attack and slow decay so that its output is around 100mV RMS for over 60dB range of input. There is also a sidetone output which is not affected by the AGC and is used to operate the VOX. R57 sets the microphone AGC threshold and dynamic range. If R57 is open circuit, the threshold is 100 microvolts and the dynamic range is 60dB; if it is 1 kilohm the values are 1mV and 40dB, and if it is 330 ohms they are 3mV and 30dB. C63 should be increased to 0.05 microfarad if R57 is 1 kilohms and to 0.15 microfarad if it is 330 ohms.

The output from the SL622C is applied to the signal input of an SL640C double-balanced modulator (IC9) whose carrier input is 8.9985 MHz or 9.0015 MHz from the carrier oscillator. The output is DSB which is applied to the 2.4kHz bandwidth 9MHz filter (F2) and one sideband removed to produce SSB (USB if 8.9985 MHz is used, LSB if 9.0015).

The RF Compressor

The SSB produced in the system above is normal SSB. Its peak/mean power ratio is fairly large, even though its mean power level is quite constant as a result of the audio AGC. It is therefore amplified in a three-stage amplifier consisting of an SL610C (IC11) followed by two SL613Cs (IC10 and IC13). The SL610C is merely to provide gain but the SL613Cs are high performance limiting amplifiers with symmetrical limiting. The signal emerging from this limiting amplifier preserves its phase information but has had practically all amplitude variation removed from it.

Such a clipped signal is rich in both harmonics and intermodulation products, so it is immediately filtered in another 2.4kHz bandwidth filter (F1) which removes both, but reintroduces some amplitude variation.

The above system is used to process all signals which are to be transmitted, in whatever mode the transmitter is operating. However if a CW signal is being sent, the first 2.4kHz filter (F2) is replaced with a 500Hz filter (F3) to ensure that a single tone is applied to the clipper. After the second filter, however, different modes are processed in different ways.

Single-sideband and CW signals are amplified in a two stage linear amplifier, applied to a 12kHz filter to remove noise and sent to the mixer via the transmit buffer.

When the transmitter is operating in AM or FM mode the clipped SSB is demodulated in an SL640C product detector (IC6) to yield clipped audio, which is then applied to the AM or FM modulators. The SSB clipping produces audio with a slightly artificial sound which, however, is not unpleasant under strong signal conditions, and is particularly easy to copy through noise.

The AM modulator is another SL640C (IC5) with carrier leak deliberately introduced so that the output is AM rather than suppressed carrier DSB. This modulator is used both in the AM and FM modes, but in the FM mode no signal is applied to the signal input and the output is an unmodulated carrier. In either case the output is amplified, filtered in the 12kHz filter (F4), and sent to the transmitter via the transmit buffer and the mixer.

In FM mode the circuit transmits an unmodulated carrier. Frequency modulation is performed off the board by using the processed audio to modulate the transceiver VFO during transmission.

The carrier on AM and FM is not, as one might expect, 9MHz. There is only one carrier oscillator on the board and it is used during transmission to produce clipped SSB. It is therefore working at 9001.5kHz or 8998.5kHz, depending on the position of the sideband selector. The AM or FM carrier is at the same frequency.

The Buffer Amplifiers

The buffer amplifiers used between the various parts of the transmitter are simple transistor or FET circuits. The first designs of the transceiver used integrated circuits to perform these functions but this led to unnecessary complexity and cost with no corresponding increase in performance.

The VOX (Voice Operated Transmit Relay)

A VOX circuit is one which switches a transceiver from receive to transmit when it detects speech at the microphone. The obvious problem with such circuits is to prevent them from reacting to signals from the loud speaker.

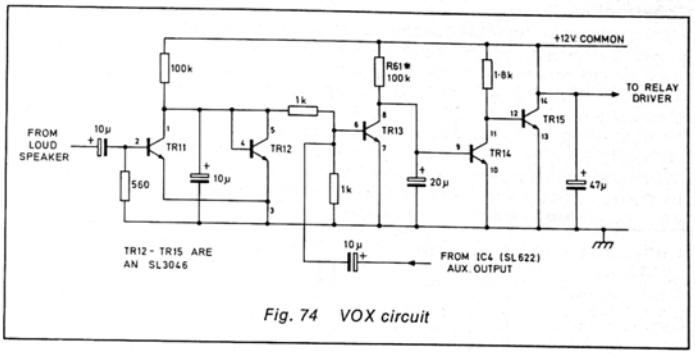


Fig. 74 VOX circuit

The simplest way to do this is to feed the loudspeaker signals to the VOX circuit so that only microphone signals which are not also present in the loudspeaker circuit affect its operation. This is quite difficult and is often liable to cause spurious switching unless the system is carefully adjusted by the operator to compensate for the microphone and the acoustics of the surroundings.

The system used in this transceiver is slightly different. The signal from the microphone is gated by the internal signal to the loudspeaker so that no input to the microphone will affect the VOX while there is a signal to the loudspeaker. The only drawback to this system is that the VOX cannot operate during the reception of non-syllabic noise. Such conditions are, however, unusual.

The circuit is shown in Fig. 74 and uses another SL3046 five transistor monolithic array. Positive half-cycles from the microphone amplifier SL622C (which is powered during reception) turn on TR13 unless prevented by the presence of a loudspeaker signal on TR11. The time constant of the gate circuit is such that VOX action can occur in the spaces between words in normal speech.

TR13 turns on TR15 via TR14. An integrator consisting of R61 and C98 controls the time which elapses between the cessation of speech and the reversion to reception. For breakthrough CW operation (when the operator listens between the dots and dashes of his own transmission) the time constant may be reduced. If the relay is a low power one it may be connected between TR15 collector and +12V, otherwise a PNP driver should be used with an input resistor in its base circuitry.

Power Supplies and Switching

The transceiver board uses three +12V supplies. One is present during reception, one during transmission, and one is common. There are three +6V integrated circuit regulators on the board, one for each +12V line, to supply the appropriate SL600s. This type of regulation greatly reduces cross-talk via the supplies.

Mode switching is accomplished by applying +12V to the relevant one of the three mode lines: CW, FM, or SSB. The two unwanted lines are earthed.

Construction

The transceiver board is constructed of double-sided printed circuit material and earth connections are made on both sides of the board – plated through holes would remove this necessity but were not used in the prototype for reasons of cost and ease of modification. As the board is very small for the complexity of circuitry it carries some of the relay connections were wired. The board diagram is Fig. 75a and the component location is given in Fig. 75b.

It would be almost impossible to make such a system stable on single-sided board but systems derived from this one and built on double-sided board should not present any particular layout problems.

Table 5 Components for the multimode transceiver (Fig. 69)

INTEGRATED CIRCUITS

IC1	SL1496
IC2	SL612C
IC3	SL613C
IC4	SL622C
IC5	SL640C
IC6	SL640C
IC7	SL612C
IC8	SL612C
IC9	SL640C
IC10	SL613C
IC11	SL610C
IC12	SL621C
IC13	SL613C
IC14	SL623C
IC15	SL630C
IC16	SL612C
IC17	SL612C
IC18	SL78L06
IC19	SL78L06
IC20	SL640C
IC21	SL78L06
IC22	SL62AC

RESISTORS (ohms)

R1	470(NOB)
R2	100(NOB)
R3	56K
R4	100
R5	47K
R6	1K
R7	10K
R8	5.6K
R9	4.7K
R10	680
R11	4.7K
R12	10K
R13	1K
R14	10K
R15	4.7K
R16	1K
R17	220
R18	220
R19	560
R20	1K
R21	50
R22	4.7K
R23	33K
R24	4.7K
R25	1K
R26	2.7K
R27	1K
R28	330
R29	10K
R30	560
R31	10K
R32	560
R33	1K
R34	10K
R35	1K
R36	1K
R37	10K
R38	1K
R39	1K
R40	1K
R41	1K
R42	4.7K
R43	330
R44	100
R45	470
R46	100
R47	470
R48	1K
R49	10K
R50	10K
R51	82
R52	10
R53	560
R54	1K
R55	1K
R56	2.2K
R57	See text
R58	470K
R59	1K
R60	100K
R61	100K
R62	1.8K
R63	15K
R64*	1K
R65*	1K
R66	4.7K(NOB)
R67†	15K

* Vertical on board
† May need selection

VARIABLE RESISTORS

RV1	10K
RV2	1K
RV3	1K
RV4	1K
RV5	10K
RV6	5K Lin.(NOB)
RV7	10K Lin.(NOB)
RV8	25K Lin.(NOB)

CAPACITORS

C1	47p
C2	0.1µF
C3	0.1µF
C4	47pF
C5	0.1µF
C6	0.1µF
C7	0.1µF
C8	4700pF
C9	0.1µF
C10	0.1µF
C11	1000pF
C12	0.1µF
C13	10pF
C14	100pF
C15	1000pF
C16	0.1µF
C17	1000pF
C18	1000pF
C19	0.1µF
C20	1000pF
C21	0.1µF
C22	1000pF
C23	1000pF
C24	0.1µF
C25	1000pF
C26	0.1µF
C27	1000pF
C28	1000pF
C29	1000pF
C30	1µF(T)
C31	1000pF
C32	0.1µF
C33	1000pF
C34	10µF(T)
C35	1000pF
C36	0.1µF
C37	1000pF
C38	1000pF
C39	1000pF
C40	1000pF
C41	0.1µF
C42	4700pF
C43	1000pF
C44	1000pF
C45	220pF
C46	50pF
C47	0.1µF
C48	1000pF
C49	4700pF
C50	0.01µF
C51	0.1µF
C52	100µF(T)
C53	0.1µF
C54	1000pF
C55	0.1µF
C56	1000pF
C57	0.1µF
C58	10pF
C59	10pF
C60	1000pF
C61	0.1µF
C62	10µF(T)
C63	4700pF
C64	330pF
C65	1000pF
C66	1000pF
C67	1000pF
C68	1µF(T)
C69	47µF(T)
C70	0.1µF
C71	1000pF
C72	100µF(T)
C73	100µF(T)
C74	1µF(T)
C75	100µF(T)
C76	47µF(T)
C77	0.01µF(T)
C78	100µF(T)
C79	0.1µF
C80	1µF(T)
C81	4700pF
C82	100pF
C83	1000pF
C84	10µF(T)
C85	47µF(T)
C86	1000pF
C87	0.5µF(T)
C88	0.1µF
C89	1000pF
C90	100µF(T)
C91	2.2µF(T)
C92	10µF(T)
C93	1000pF
C94	1000pF
C95	1000pF
C96	10µF(T)
C97	0.1µF
C98	20µF(T)
C99	10µF(T)
C100	0·1µF(NOB)
C101	1000µF(NOB)
C102	100µF(T)
C103	1000pF
C104	1000pF
C105	10µF(T)
C106	15pF(SOT)
C107	4.7nF

NOB = Not on board
All ¼W film types
Tolerance 5%

SOT = Select on test

All capacitors except C101 (which is aluminium electrolytic) are either bead tantalum (marked T) or miniature ceramic; tolerance 20%

Table 5 (continued)

TI	6:1 Toroidal RF transformer
L1	3.1µH Nominal, slug tuned screened RF coil.
L2	550µH Nominal, slug tuned screened RF coil.
L3	370µH Nominal, slug tuned screened RF coil.
F1	XF9-B
F2	XF9-B
F3	XF9-M. KVG crystal filters
F4	XF9-E
X1	8545KH
X2	9001.5KHz Parallel (30p) resonant
X3	8998.5KHz HC18 or HC25 crystals
X4	9001Khz

RL1–6 National R5-12V miniature relays

Diode ring – Anzac MD108

TRANSISTORS

TR1–5	SL3046C
TR6–10	SL3046C
TR11–15	SL3046C
TR16–17	SL301C Dual transistor
TR18	2N3906 or similar PNP
TR19	2N3819 or similar N-FET
TR20	2N3819 or similar N-FET
TR21	2N918 or similar fast NPN
TR22	2N706 or similar NPN
D1–8	1N914 or similar low capacity Si switching diode
D9	MV1 1
D10–11	MBD101
D12	1N914

Delay line
Belfuse 0420-0400-05, or any delay line with 500 ohm ports, 300 to 800ns delay and less than 8dB insertion loss at 9MHz.

Fig. 75a Multimode transceiver PCB

Fig. 75b Multimode transceiver component layout

27MHz AM/SSB transceiver

Fig. 76 shows the circuit diagram of a dual converion AM/SSB transceiver intended for use on 27MHz Citizens' Band. It has evolved from the versatile multimode transceiver described above but where the multimode transceiver is optimised for performance, this transceiver, being primarily intended for the CB market, is optimised for economy.

Like the multimode transceiver, this system is equipped with a noise blanker but instead of a delay line uses a low-cost ceramic 10.7MHz IF filter (which also acts as the first IF filter) as the delay element. The filter has a delay of about 1.5 microseconds.

The receiver is conventional. A 27MHz tuned circuit is followed by an SL1610C RF amplifier and an SL1641C mixer to the first IF of 10.695MHz. After a 10.695MHz filter (which also acts as a noise blanker delay) the signal passes through an SL1496C noise gate and on to the SL1641C second mixer. The noise blanker receiver is driven at 27MHz by the SL1610C RF amplifier and consists of an SL1613C amplifier and detector followed by a CMOS 4011 acting as a monostable to generate the blanking pulse to the SL1496C.

The output from the second mixer, at 455kHz, is switched by diode switches to one or other of two ceramic ladder filters – one with 2.4kHz bandwidth for SSB and the other with 6kHz bandwidth for AM. The IF strip following the filter consists of an SL1611C and two SL1612Cs and contains a simple ceramic filter to minimise broadband noise. An SL1623C AM/SSB detector is used which generates AGC during AM reception and an SL1621C generates AGC during SSB reception.

Squelch is obtained from the AGC line by an SL748C op. amp. acting as a threshold switch. Its output switches the audio path by turning on and off the bias to a transistor amplifier. The audio output stage uses a TBA800 3 watt integrated circuit audio amplifier.

The transmitter uses an SL1626C as a microphone AGC amplifier and an SL1641C as either an AM modulator or as a DSB generator, depending on switching. The 455kHz AM or DSB is passed through the appropriate filter and mixed to 10.695MHz, where it is refiltered and mixed again to its final 27MHz frequency. Both mixers are SL1600 devices – the SL1640C and the SL1641C respectively.

The transceiver, like the others described above, requires the addition of oscillators, an RF power amplifier and power supplies. It is intended for use with the Plessey SP8921/8922 CB synthesiser but also requires an oscillator which may be switched between 453.5kHz, 455kHz and 456.kHz for use as the receiver BFO and the carrier oscillator in the transmitter.

Power supplies of +6V and +12V are required, which are switched in various ways during transmission and reception. All supplies must be well decoupled at HF and LF.

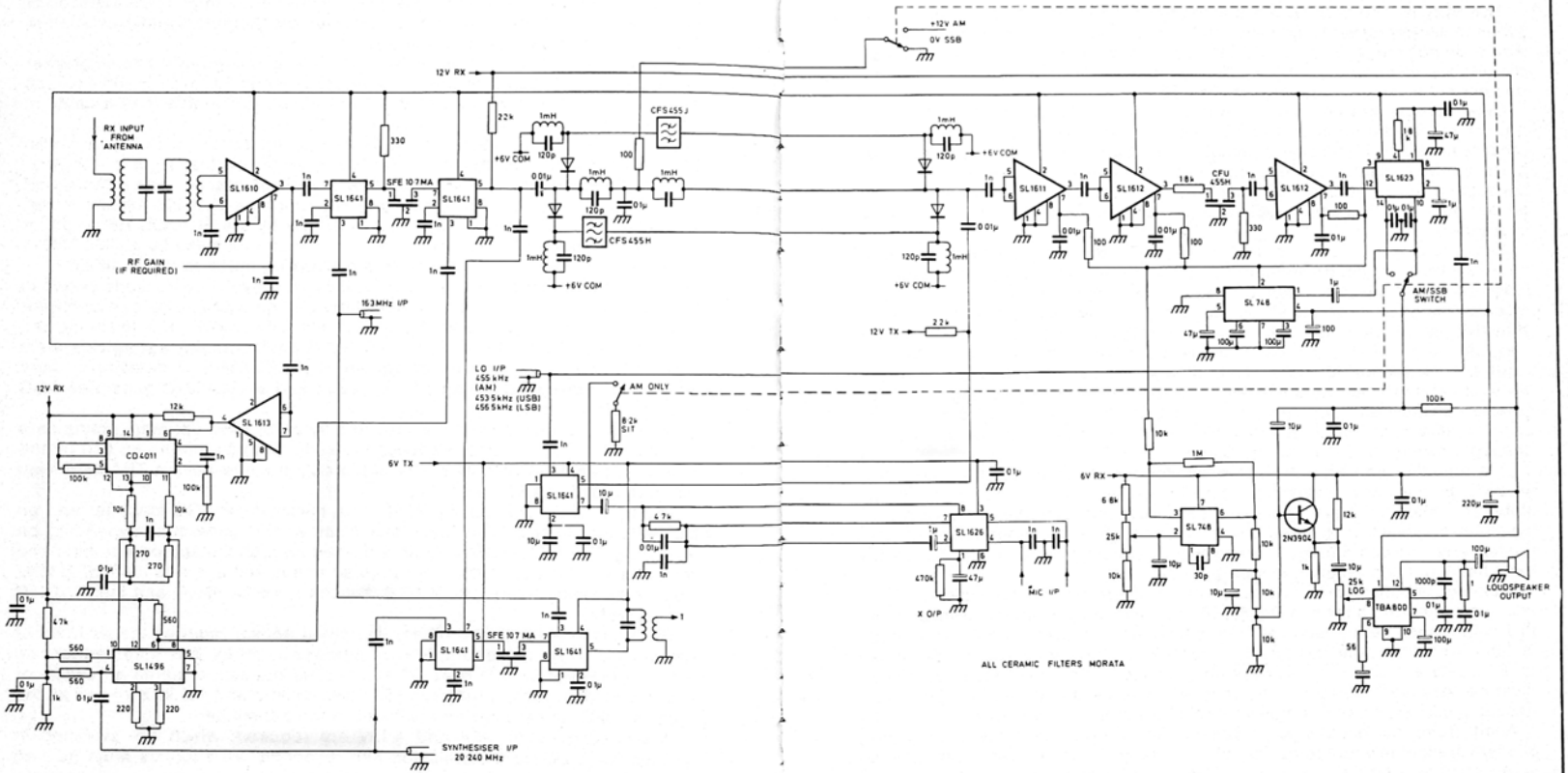


Fig. 76 Dual conversion AM/SSB Citizens' Band transceiver

NBFM receiver IF/detector

The SL664C and SL665C are intended for use in NBFM receivers as amplifier/detector/squelch modules and, of course, the SL664 also has an audio output stage. Full circuit diagrams of normal applications of these circuits are given in Figs. 77 and 78 respectively. Printed circuit layouts and component placings are shown in Figs. 79 and 80.

Other layouts can be used but it is important to keep signal tracks short and to isolate the input and output leads of amplifiers from each other to prevent feedback. Other points which should be remembered are to keep as much earth conductor as possible and to keep all leads carrying HF, even decoupling leads, as short as possible. The best layouts use double-sided printed boards with a continuous ground plane on the component side – this undoubtedly helps stability.

The circuits, having a low power consumption and limiting amplifiers, have no resistance to intermodulation although they have excellent dynamic range and must be used after the main selectivity of the receiver. Modern receiver design emphasises strong signal performance even at the expense of sensitivity and hence front ends having much gain are not popular. This can leave an uncomfortable gap between the two to four microvolts output from a receiver filter and the 10 microvolts or so required by these circuits to give an adequate signal/noise ratio. Redesign of the front end to give slightly more gain is possible and certainly the easiest solution but it may produce an unacceptable reduction in intermodulation performance. An amplifier is then needed between the filter and the SL664/5.

This amplifier can also provide a convenient matching for the filter but, preceding as it does a very high gain integrated circuit, it can suffer from stubborn instability. It also increases the power consumption of the receiver which is annoying in a hand-portable, although a hand-portable with its limited antenna can usually tolerate a higher gain front end and hence is least likely to need an extra stage of IF gain.

Suitable amplifiers may be made with a single bipolar transistor or FET and two circuits are shown in Fig. 81. The FET circuit uses more current and an FET with a good performance at 1mA is needed. The bipolar transistor circuit is far less demanding but has a lower input impedance (which depends on DC, beta and C_{ob} and will vary from device to device). These amplifiers must be very well isolated if the receiver is to be stable and the powerful decoupling of the bipolar transistor circuit is a point in its favour.

Apart from the occasional necessity for a low-gain preamplifier, the SL664/5 present few problems and are very easy to use. As mentioned above some care must be paid to layout to isolate input and output, particularly at the same frequency, as much as possible. Other points to be remembered are the use of non-inductive capacitors (many capacitors are inductive rather than capacitive at frequencies of only a few MHz) and adequate decoupling of all bias points and power supplies. In connection with this it is worth remembering that it is useless to use a good RF capacitor; with short leads if the printed connection to it is long and narrow.

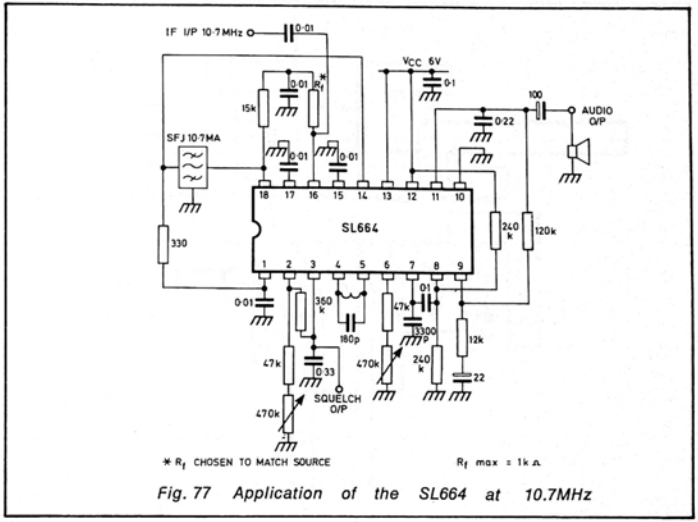


Fig. 77 Application of the SL664 at 10.7MHz

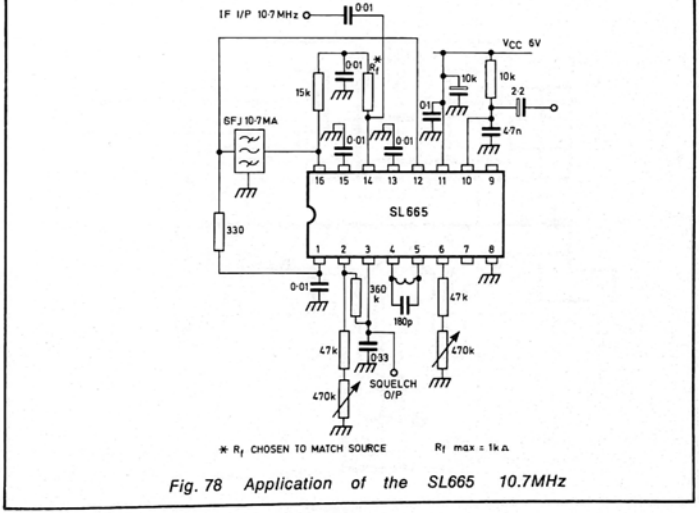


Fig. 78 Application of the SL665 10.7MHz

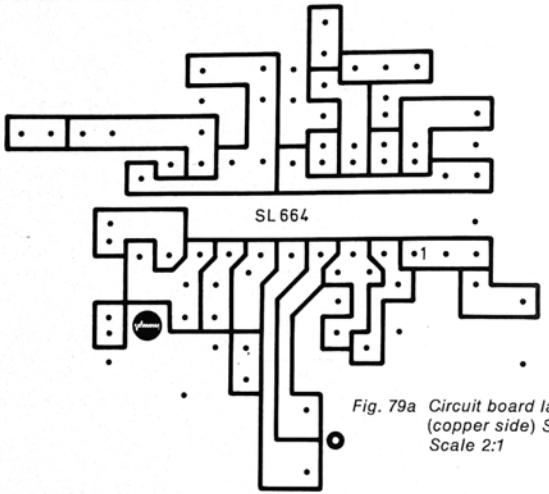


Fig. 79a Circuit board layout (copper side) SL664. Scale 2:1

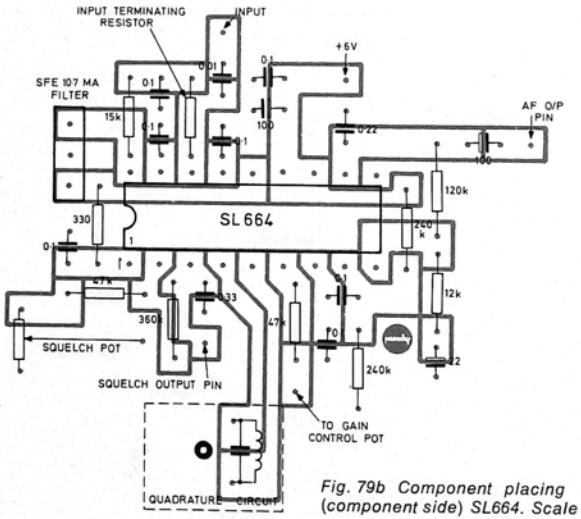


Fig. 79b Component placing (component side) SL664. Scale 2:1

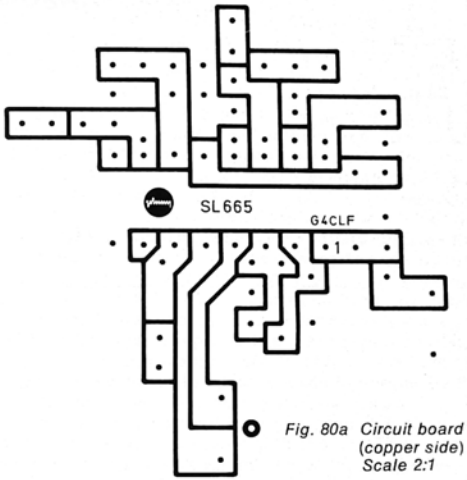


Fig. 80a Circuit board layout (copper side) SL665. Scale 2:1

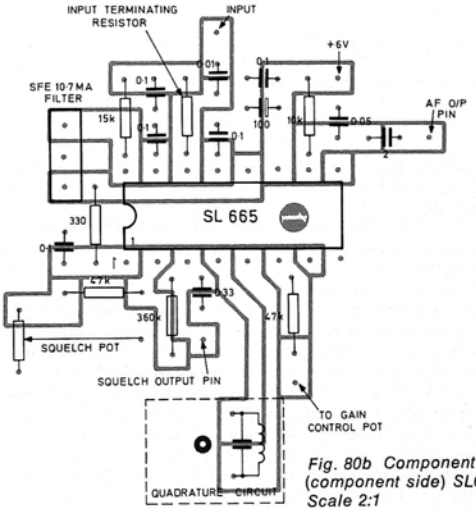


Fig. 80b Component placing (component side) SL665. Scale 2:1

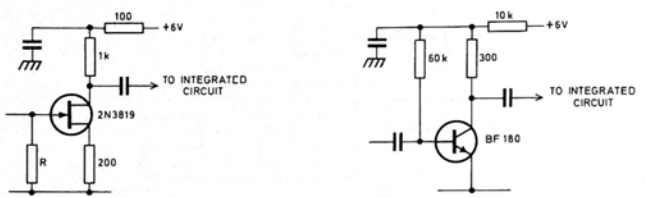


Fig. 81 FET and bipolar buffer amplifiers

Citizens' Band synthesiser using the SP8921/8922

The SP8921/22 combination is intended to synthesise the frequencies required in a 40-Channel Citizens' Band transceiver. The 40 channels are spaced at 10kHz intervals (with some gaps) between 26.965 and 27.405MHz. Local oscillator frequencies for the reception of these channels with intermediate frequencies of 455kHz, 10.240MHz, 10.695MHz and 10.700MHz are also synthesised. Table 6 shows the relationship between the program input and the channel selected. By using a program other than one of the 40 given other frequencies may be selected – in fact there are 64 channels at 10kHz separation available from 26.895 to 27.525MHz and programming starts at all zeros on inputs A through F for 26.895 and each increase of one bit to the binary number on these inputs increases the channel frequency by 10kHz until all '1's give 27.525MHz. The A input is the least significant bit, F the most significant. The programming input on pin 16 of the SP8922 is normally kept high but making it low increases the programmed frequency by 5kHz. Table 7 shows the programming required to obtain various offsets.

The circuit diagram of a CB synthesiser is shown in Fig. 82. It is intended for use in double conversion receivers with IFs of 10.695 and 455kHz and generates either the frequency programmed or the frequency programmed less 10.695MHz.

If other offsets are programmed the connections to pin 15 of the SP8921 and pin 2 of the SP8922 must be altered according to Table 7.

The synthesiser consists of the SP8921 and the SP8922 plus an SP1648 voltage controlled oscillator.

The programming inputs to the SP8922 are as shown in Table 6. Logic '1' is +3V or more, logic '0' is either ground or an open circuit. The circuit diagram of a programming input port is shown in Fig. 83. If a switch, constructed so as to select the correct combination for each channel, can be obtained this is the obvious way to program the synthesiser; otherwise a ROM may be suitably programmed and placed between the switch and the SP8922.

The crystal oscillator in the SP8921 is trimmed by a small variable capacitor, C3, which must be set up during alignment of the synthesiser so that the output frequency on pin 4 is 10.240000MHz. The only other adjustment is to set the core of L1 so that the varicap control voltage is 2.85V when the synthesiser is set to channel 30 transmit. Since the difference between transmit and receive frequencies is over 10MHz it is not possible to tune both with the same tuned circuit and an extra capacitor is switched by means of a diode during reception.

The phase/frequency comparator of the SP8921 can have an output swing from 0.5V to 3.8V but it is better to work in the range 1.5V to 3.0V as the phase-error output voltage is more linear in this region. The ZC822 tuning diode specified for this synthesiser may be replaced by any other tuning diode provided it will tune the VC0 over the required range, or a little more, as the control voltage goes from 1.5 to 3.0V. With slight coil changes the MV2105 has been used successfully in this synthesiser.

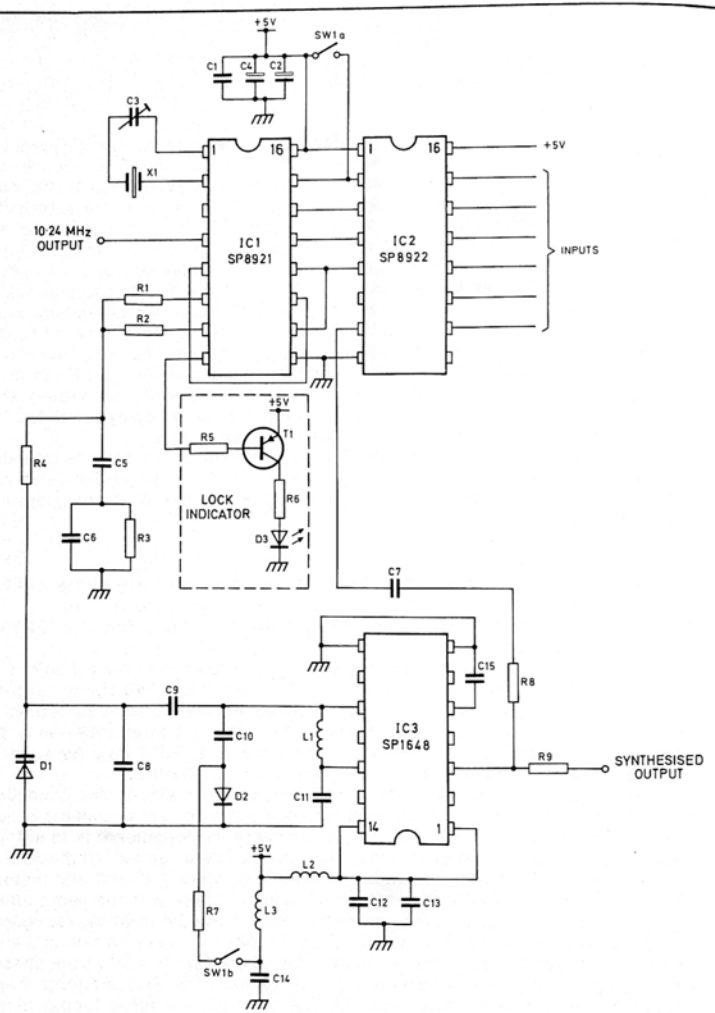


Fig. 82 Low cost CB synthesiser component layout

All resistors are in ohms and $\frac{1}{8}$W ± 10% unless otherwise stated. Capacitor values are in microfarads unless otherwise stated.

IC1	SP8921
IC2	SP8922/SP8923 – 40 channel
IC3	SP1648
T1	2N 3906
D1	ZC822, Ferranti varactor diode
D2	1N4148 Silicon diode
D3	LED lock indicator
X1	10.240MHz crystal, series mode
L1	11 turns 30 gauge cotton covered wire on Neosid A7 assembly
L2	100 microhenries RF choke
L3	100 microhenries RF choke
R1	1.0k ± 5%
R2	1.0k ± 5%
R3	8.2k ± 5%
R4	33k
R5	10k
R6	150 (adjust for LED brightness)
R7	1k
R8	1k
R9	470 (adjust for required output level)
C1	0.1
C2	100, 10V solid tantalum
C3	2 – 22pF variable
C4	100, 10V solid tantalum
C5	1,10V solid tantalum
C6	0.1
C7	1000pF
C8	22pF + 10%
C9	0.01
C10	100pF ± 10%
C11	0.01
C12	0.1
C13	10,10V solid tantalum
C14	0.1
C15	1000pF
SW1	2 pole, 1 way switch, (receive/transmit)

Channel No.	Input Code F E D C B A	Output frequency with R/T = 0 (MHz)
1	0 0 0 1 1 1	26.965
2	0 0 1 0 0 0	26.975
3	0 0 1 0 0 1	26.985
4	0 0 1 0 1 1	27.005
5	0 0 1 1 0 0	27.015
6	0 0 1 1 0 1	27.025
7	0 0 1 1 1 0	27.035
8	0 1 0 0 0 0	27.055
9	0 1 0 0 0 1	27.065
10	0 1 0 0 1 0	27.075
11	0 1 0 0 1 1	27.085
12	0 1 0 1 0 1	27.105
13	0 1 0 1 1 0	27.115
14	0 1 0 1 1 1	27.125
15	0 1 1 0 0 0	27.135
16	0 1 1 0 1 0	27.155
17	0 1 1 0 1 1	27.165
18	0 1 1 1 0 0	27.175
19	0 1 1 1 0 1	27.185
20	0 1 1 1 1 1	27.205
21	1 0 0 0 0 0	27.215
22	1 0 0 0 0 1	27.225
23	1 0 0 1 0 0	27.255
24	1 0 0 0 1 0	27.235
25	1 0 0 0 1 1	27.245
26	1 0 0 1 0 1	27.265
27	1 0 0 1 1 0	27.275
28	1 0 0 1 1 1	27.285
29	1 0 1 0 0 0	27.295
30	1 0 1 0 0 1	27.305
31	1 0 1 0 1 0	27.315
32	1 0 1 0 1 1	27.325
33	1 0 1 1 0 0	27.335
34	1 0 1 1 0 1	27.345
35	1 0 1 1 1 0	27.355
36	1 0 1 1 1 1	27.365
37	1 1 0 0 0 0	27.375
38	1 1 0 0 0 1	27.385
39	1 1 0 0 1 0	27.395
40	1 1 0 0 1 1	27.405

Table 6 SP8922/1 O/P frequencies with 10.240 crystal (0 = contact open, 1 = contact closed to Vcc)

Offset	SP8921	SP8922
0	0	0
–455kHz	0	1
–10.240MHz	1	0
–10.695MHz	1	1

Table 7

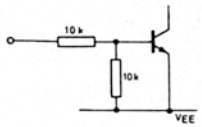


Fig. 83 Program input circuit

The low pass filter of the PLL consists of C5, C6 and R3. If faster lock (at the expense of larger noise and reference sidebands) is required the filter may be redesigned. If the synthesiser is used in a scanning receiver, a switched filter should be used to give fast lock during scanning but a slower lock and cleaner signal during normal operation. The lock output on pin 8 of the SP8921 is used to light an indicator when the loop is *not* locked and should also be used, in a transmitter or transceiver, to prevent transmission when the loop is unlocked.

Fig. 84 shows the circuit board layout and component placing of this synthesiser. It requires a single +5V supply and draws about 60mA. The component list is given in Table 8. The performance is improved if double-sided board is used with a ground plane on one side. A small further improvement would come from the use of a grounded screening can over the whole system.

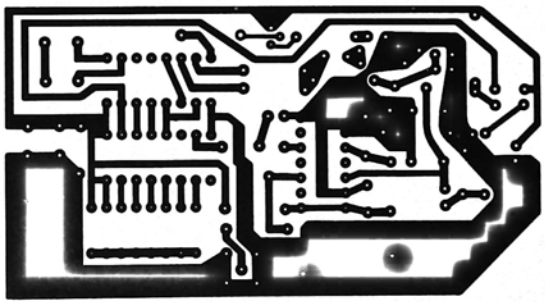


Fig. 84a Printed circuit layout for CB synthesiser

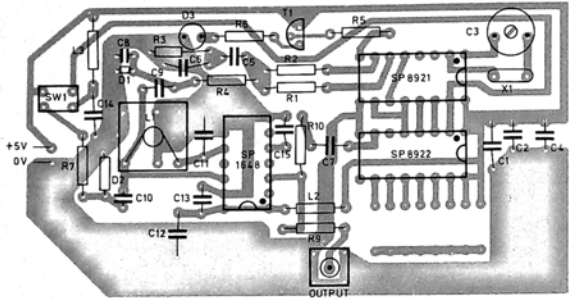


Fig. 84b PCB component layout for CB synthesiser

The synthesiser has reference frequency sidebands 50dB down at 1.25kHz from the carrier. All output over 5kHz from the carrier is over 70dB down. Lock time for a change from channel 0 to channel 40 (a frequency change of 440kHz) is around 35ms. Photographs of the output spectrum and the change of control voltage with time during a step from channel 0 to channel 40 are shown in Fig. 85. Stepping from transmit to receive or vice versa takes somewhat longer because of the much larger change of frequency but is generally complete within 75ms.

This synthesiser is quite basic but has adequate performance for the majority of CB applications. If improved performance is required there are two possibilities; an improved FET oscillator having lower floor noise instead of the SP1648 or an improved low pass filter to reduce reference frequency sidebands. Fig. 86 shows the circuit diagram of an improved oscillator using an E304 FET and the same coil and varactor as in the simple synthesiser. Fig. 87 shows a high performance synthesiser using an FET oscillator, a twin-T filter in the VCO control line to reduce reference sidebands at 1.25kHz to below —90dB, an SL1610C buffer giving over 60dB isolation from the output line back into the VCO, and separate voltage stabilisers for the oscillator and the logic of the system.

Fig. 88 shows a block diagram of the use of the synthesiser in a typical double conversion 27MHz Citizens' Band transceiver with direct generation of the transmit frequency. In such a system it is essential that the power amplifiers in the transmitter are well isolated from the VCO, otherwise phase modulation and quite unacceptable splatter will occur.

To reduce the need for isolation the system shown in Fig. 89 may be used – the synthesiser runs with an offset of 10.240MHz duringt ransmission and this signal is mixed with the 10.240 signal from the synthesiser to produce the final 27MHz for transmission. Such a transmitter is less liable to phase modulation resulting from inadequate screening but the output of the mixer must be well filtered to prevent transmission of the difference of 16.3MHz and 10.240MHz as well as their sum.

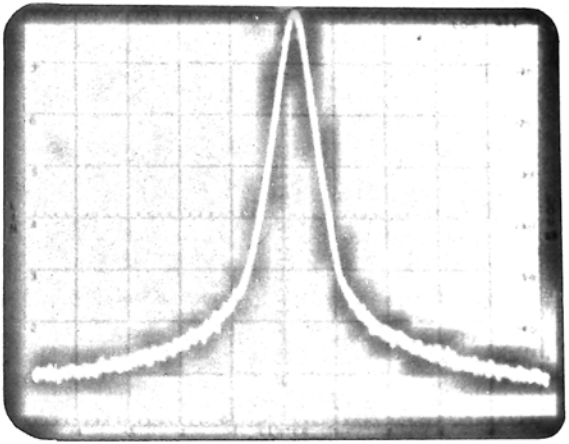


Fig. 85a Typical output spectrum of basic synthesiser (Vert.:16dB/div.,Horiz.: 2kHz/div.,) BW:300Hz, fo:27.065MHz

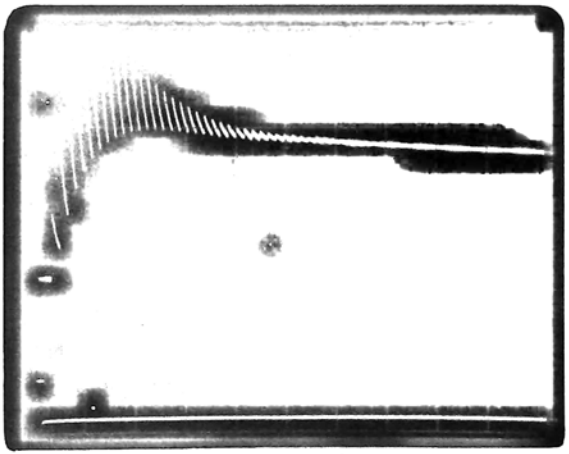


Fig. 85b Typical transient response of basic synthesiser. Response of varactor line to step program change 1–40. Vert.:200mV/div.,Horiz.:5ms/div. N.B. Droop of response is due to the measuring instrument being AC-coupled.

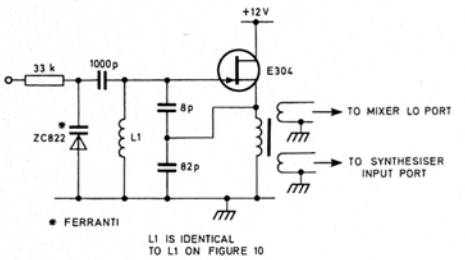


Fig. 86 FET voltage controlled oscillator for 27MHz Citizens' Band Synthesiser

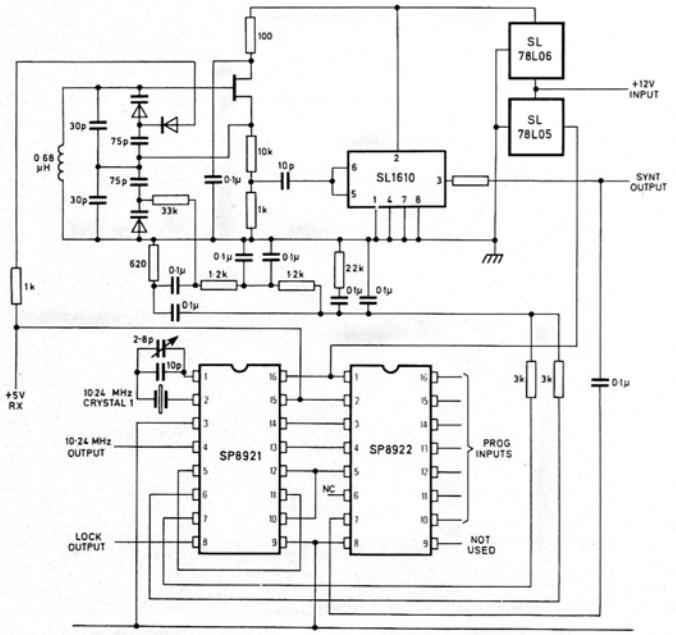


Fig. 87 High performance Citizens' Band synthesiser

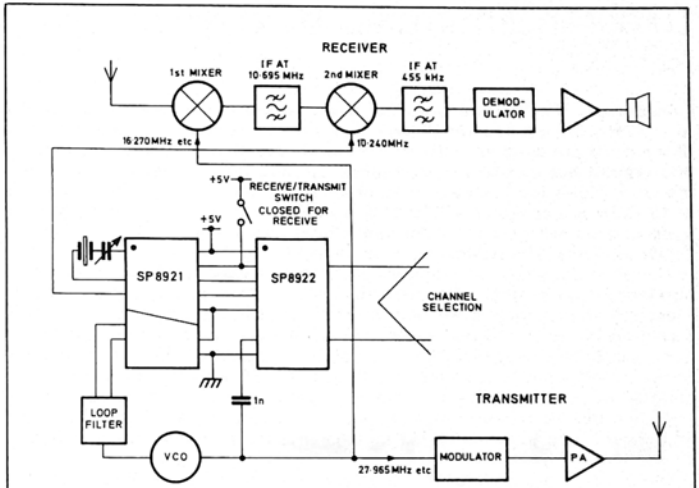


Fig. 88 Typical double converion set for Citizens' Band using the SP8921 (Direct generation of transmit frequency)

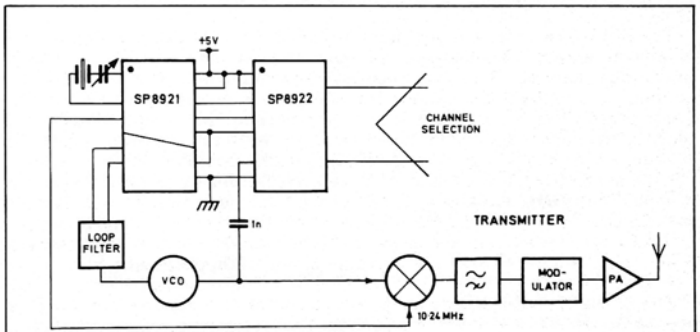


Fig. 89 Typical Citizens' Band transmitter using the SP8921 (Indirect generation of transmit frequency)

European 2m amateur band synthesiser

In Europe, the '2-metre' Amateur Band covers frequencies from 144MHz to 146MHz. Different countries have their own conventions about which parts of the band are used for different modes of operation. Some are internationally agreed but all use 25kHz channel spacing for channelised FM, unlike the USA where the standard is 15 or 30kHz. If low side injection and an IF of 10.7MHz are chosen the SP8921 and SP8922 CB synthesiser chips may be used to generate local oscillator frequencies over the whole 2 metre band at 25kHz intervals. The basic system is shown in Fig. 90.

This note does not describe the VCO because various types are available and there is no general agreement as to which is the best for the purpose. At Plessey Semiconductors we built the system using a very low noise, high stability VCO using a Surface Acoustic Wave (SAW) delay line but this technology is only just available and is not yet competitive in amateur applications. Probably the best system would use an FET 'Kalitron' oscillator with a buffered output both to the transceiver mixer and to the divider input, but in any case the VCO should have as little noise and phase jitter as possible and should tune from about 133 to 135.6MHz for a tuning voltage range of 1.5V to 3V.

The divider uses an SP8622 ÷5 prescaler followed by the SP8921 and the SP8922. The SP8921, also contains the crystal oscillator and its associated divider and the phase/frequency comparator.

The SP8622 is an easily-used circuit. It requires an input AC level of between 400 and 800 mV p–p and has two bias points which should be decoupled to ground with 0.1 microfarads as should its supply. Its input and output connections are made via 1000pF capacitors. No precautions against self-oscillation are necessary in this application as an input should always be present.

The SP8922 receives a signal from the SP8622 and is used to program the channel required. Table 8 shows the inputs required on pins 10 to 16 (A to G) for various channels. Pin 2 (the Receive/Transmit pin in 27MHz CB operation) is connected to the supply. Since the SP8922 was not designed for amateur 2-metre use there is no simple relationship between the program inputs and the channel selected so either complex switch wiring or a read only memory is required. A commercial ROM or a diode matrix could be used.

If the synthesiser is used in a transmitter it is necessary to mix a frequency-modulated 10.7MHz signal with its output and filter the image. If the transmitter is to be used with repeaters the ROM (or switch) must contain logic to provide a 600kHz shift between transmission and reception. The connections between the SP8922 and the SP8921 are made as in the CB application.

The SP8921 is used exactly as in the 27MHz CB application except that pin 15, the Receive/Transmit pin is grounded. The crystal frequency is 10.240MHz and the low-pass filter in the phase comparator is the more complex of the two described previously in order to reduce 1.25kHz reference frequency sidebands in the synthesiser. The filter should be shielded both from the dividers and the VCO to obtain best performance. The lock output on pin 8

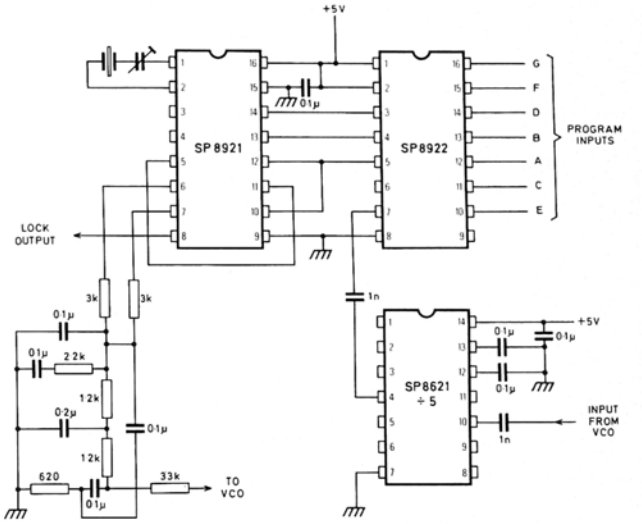


Fig. 90 Divider and filter for synthesiser for 2 metre amateur band

should be connected to prevent transmission when the synthesiser is unlocked. In transmitters, the VCO should be very well shielded from the PA stages to prevent interference and unlocking due to feedback.

If the synthesiser is required to interpolate between the 25kHz channels, the crystal oscillator in the SP8921 should be replaced by two crystal oscillators – one to synthesise the channels accurately and the other, a variable crystal oscillator with a tuning control (possibly using a varactor) used to interpolate or provide Receiver Incremental Tuning (RIT). It is better to use external oscillators than try to make the SP8921 switch between these two functions.

The performance of the synthesiser is good – reference sidebands can be reduced to —90dB on the signal and there are no spurious outputs visible on a 100dB spectrum analyser but care is needed to shield and decouple the various parts and their power supplies. The ultimate spectral purity of the output not only depends on the synthesiser but also on the baseband noise of the VCO used.

Transceiver Frequency (MHz)	Channel	Actual Synthesiser Frequency (MHz)	Pin Number						
			16 G	12 A	13 B	11 C	14 D	10 E	15 F
145.000	SO[RO(T)]	134.300	0	0	1	0	1	0	1
145.025	R1(T)	134.325	1	0	1	0	1	0	1
145.050	R2(T)	134.350	0	1	1	0	1	0	1
145.075	R3(T)	134.375	1	1	1	0	1	0	1
145.100	R4(T)	134.400	0	0	0	1	1	0	1
134.125	R5(T)	134.425	1	0	0	1	1	0	1
145.150	R6(T)	134.450	0	1	0	1	1	0	1
145.175	R7(T)	134.475	1	1	0	1	1	0	1
145.200	R8(T)	134.500	0	0	1	1	1	0	1
145.225	R9(T)	134.525	1	0	1	1	1	0	1
145.250	R10(T)	134.550	0	1	1	1	1	0	1
145.500	S20	134.800	0	0	0	1	0	1	1
145.525	S21	134.825	1	0	0	1	0	1	1
145.550	S22	134.850	0	1	0	1	0	1	1
145.575	S23	134.875	1	1	0	1	0	1	1
145.600	S24 [RO(R)]	134.900	0	0	1	1	0	1	1
145.625	R1(R)	134.925	1	0	1	1	0	1	1
145.650	R2(R)	134.950	0	1	1	1	0	1	1
145.675	R3(R)	134.975	1	1	1	1	0	1	1
145.700	R4(R)	135.000	0	0	0	0	1	1	1
145.725	R5(R)	135.025	1	0	0	0	1	1	1
145.750	R6(R)	135.050	0	1	0	0	1	1	1
145.775	R7(R)	135.075	1	1	0	0	1	1	1
145.800	R8(R)	135.100	0	0	1	0	1	1	1
145.825	R9(R)	135.125	1	0	1	0	1	1	1
145.850	R10(R)	135.150	0	1	1	0	1	1	1

Table 8 Programming for 2-metre synthesiser

VHF/UHF synthesisers using 2-modulus prescalers

Fig. 91 shows the divider for a synthesiser operating between 100MHz and 199.9875MHz with 12.5kHz channel spacing. Fig. 92 shows the divider for a similar synthesiser operating between 300MHz and 512MHz with 25kHz channel spacing. The limit of operation of the SP8647 decade is defined in the datasheet as 250MHz giving a top frequency of 500MHz but since nearly all SP8647 devices will, in fact, operate at 256MHz, the figure given is quite conservative in practice.

Both synthesisers are designed to use a reference frequency of 12.5kHz.

The VHF divider uses an SP8690 ÷10/11 counter combined with an SP8794 modulus extender to give a ÷80/81 two-modulus counter. The output from this counter at the highest input frequency is about 2.5MHz so the remaining counters may use CMOS logic operating on a 10V rail (operation below 10V might be possible but 5V operation would not).

The programmable counter consists of five CD4029 4-bit binary/decade counters, one used in binary mode and the rest either as decades or in modes where the matter is irrelevant. The counters are operated in the synchronous mode, where the output of the SP8974 (which requires a 33k ohm resistive pullup to the CMOS positive supply) drives the clock inputs of all the counters and the 'clock enable' inputs are cascaded.

Counters X1 and X2 form the counter controlling the two-modulus prescaler and count down from the number pre-set into them by the '12.5s of kHz' and '100s of kHz' inputs until they reach zero; the SP8690/8794 combination then stops dividing by 81 and divides by 80. X1 and X2 stop counting until the next cycle starts. It is important that the propagation delay from the output of the SP8974, via this counter, back into the control input of the SP8974 is shorter than a count cycle of the SP8690/8794 combination, otherwise the counter will not control the two-modulus counter soon enough to prevent the next cycle of the two-modulus counter being 81 instead of 80. At 200MHz this means that the propagation delay around the loop must be less than 700ns.

Counters X3, X4 and X5 form the MHz, 'tens of MHz', and 'hundreds of MHz' counters respectively. X5 is hard-wired to count one only so that the system will only work between 100MHz and 199.9875MHz; if lower frequency operation is required this counter could be made programmable but the X3/ X4/ X5 counter must not be allowed to operate with a division ratio less than 80, otherwise the two-modulus part of the system can not be operated over its full range (as described in section 2) and the synthesiser will malfunction. This places an absolute limit on the low frequency operation of the divider of 80MHz. The upper limit of 200MHz is set by the speed of the SP8690 and the CMOS.

All the CMOS counters operate in the 'countdown mode'. When the X3/X4/ X5 counter reaches zero all five counters are again preset to the values programmed on their input. The inverter on the output of X5 drives all the 'preset' inputs and if the preset time of all the counters is similar should perform the function perfectly well.

If, however, some counters preset more quickly than others it is possible that the signal on the 'preset' line may disappear before the operation is

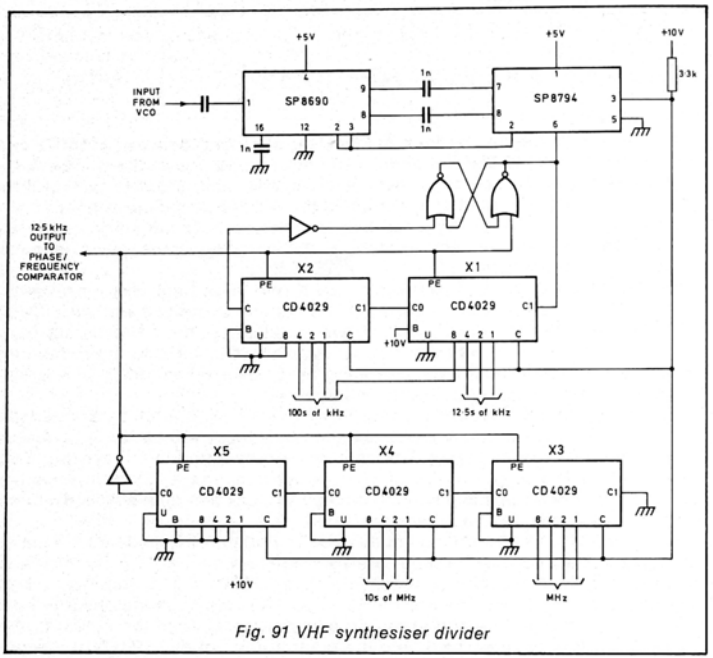


Fig. 91 VHF synthesiser divider

complete in all counters. In that case the inverters could be replaced with a monostable or some other form of pulse extender but it is essential that the preset pulse ends before the next clock pulse arrives. In other words, the delay from the edge of the clock pulse which reduces the counter to zero to the end of the preset pulse must not exceed 350ns.

The program inputs, with the exception of the 12.5s of kHz are programmed in binary coded decimal. The 12.5s of kHz are programmed in 3 bits of binary code. Each input must be connected to either +10V or to ground so either 2 way programming switches or pulldown resistors must be used.

The operation of the UHF synthesiser is very similar except that TTL is used instead of CMOS and a ÷2 fixed-modulus prescaler precedes the two-modulus counter. The prescaler is necessary because although ÷10/11 counters are available which will count at over 600MHz the SP8790 modulus extender will not operate with an input frequency of over 40MHz which limits the ÷10/11 counter input to 400MHz. The use of this fixed prescaler means that the reference frequency is 12.5kHz although the channel spacing is 25kHz.

The ÷2 prescaler is unnecessary and a reference frequency of 25kHz may be used if the modulus extender is built with ECL10K logic, which allows it to operate at up to 51.2MHz input frequency. If this is done the SP8647

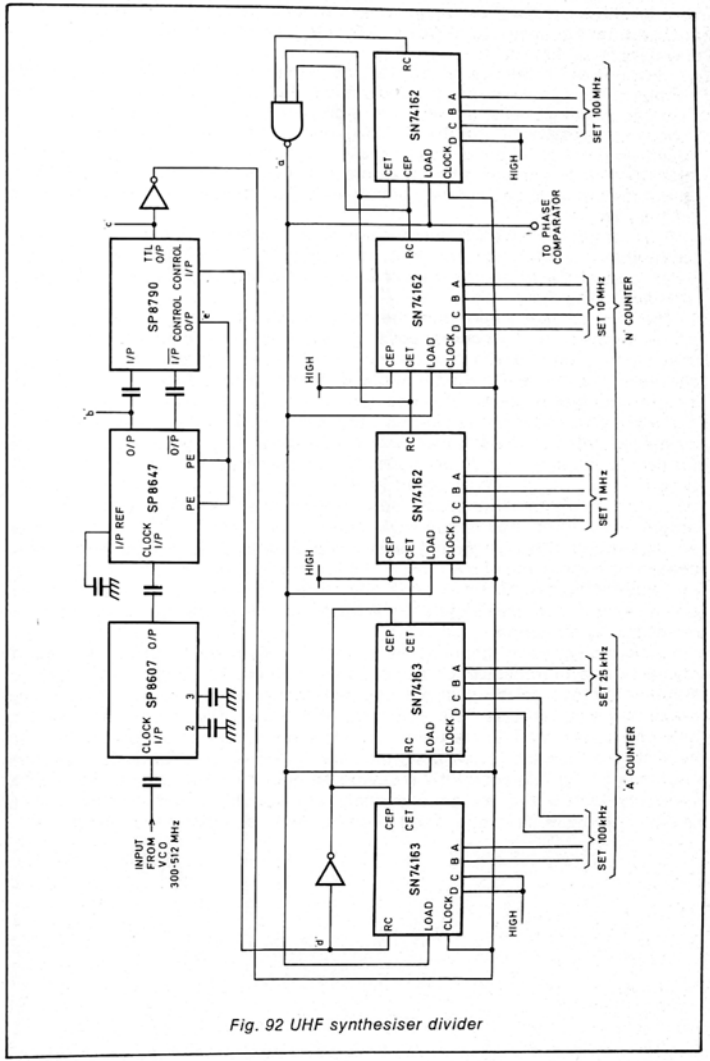


Fig. 92 UHF synthesiser divider

÷10/11 counter must be replaced with a faster counter such as the SP8685. Apart from the necessary ECL10K/TTL interface circuits the remainder of the system is unchanged.

The use of TTL allows all logic to use the same +5V supply but introduces complications in programming and choice of counter. There is no TTL device similar to the CD4029, so separate 4-bit binary and BCD counters must be chosen, the SN74163 and the SN74162 respectively. These counters may be used synchronously but the carry enable system is more complex than that of the CD4029. In addition since they are not reversible counters they must be programmed in 9s complement binary or 9s BCD instead of the simpler codes of the CMOS.

The remainder of each synthesiser would consist of a phase/frequency comparator, a reference frequency generator and VCO. The reference oscillator, part of the reference divider and the phase comparator could well be realised using the SP8760.

The method used to program the dividers will vary witht he use to be made of the synthesiser. If a general coverage synthesiser is required all the inputs may be programmed with thumbwheel switches. Logic may be placed between the switches and the programmable counters to introduce offsets if direct programming of receiver local oscillators is required.

If a few pre-programmed channels are required, a read only memory should be placed between the channel switch and the synthesiser. The simplest ROM for this application is a diode matrix. This has the advantage that it is easily programmed and re-programmed in the field but it is somewhat bulky. If a number of equipments are required with the same chanelling a commercially programmed integrated circuit ROM may be used and in intermediate cases an ultra-violet erasable PROM is suitable. Since most mobile radio transceivers operate much of the time in duplex mode (transmit on one frequency and receive on another) it is generally more convenient to program transmit and receive frequencies separately in the ROM than to arrange logic to provide offset during reception.

Traditionally, each channel in a mobile transceiver used two quartz crystals – one for transmission and one for reception. As standards of frequency stability improve so the cost per channel continues to rise. By using a high performance synthesiser with counters of the type described in this section only one quartz crystal is required per transceiver, no matter how many channels are synthesised. Such a synthesiser is economic with as few as three channels taking into account the saving on quartz crystals alone. Savings on inventory (since the reference crystals are standard) and commonality of design can make its use justified even in single channel transceivers.

Appendices

Appendix A Pin connections and DC voltage tables

Appendix B Low noise basics

Appendix C Characteristics and interfacing for the SP8000 series high speed dividers

Appendix D Using the SL652 as a stable tone source and as an FSK modem

Appendix E Input characterisation for the SP8000 series

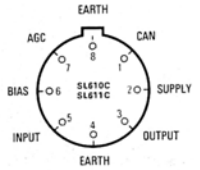
Appendix F The use of hybrid IC front end amplifiers to improve the sensitivity of SP8000 series high speed dividers

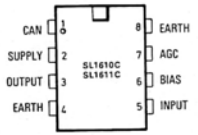
Appendix A

Pin connections and DC voltage tables

SL610C/11C @ +6V supply

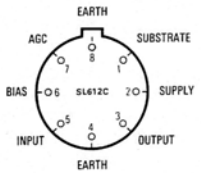
Pin	Voltage
1	Ground
2	+6V
3	1.6V
4	Ground
5	0.85V
6	0.85
7	Externally applied
8	Ground

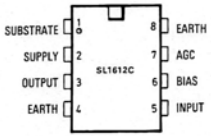




SL612C

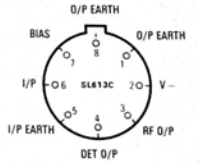
Pin	Voltage
1	Ground
2	+6V
3	1.9V
4	Ground
5	0.75V
6	0.75V
7	Externally applied
8	Ground

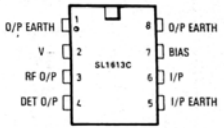




SL613C

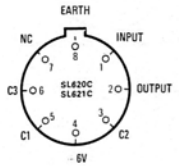
Pin	Voltage
1	Ground
2	Supply
3	2.0V
4	Depends on load
5	Ground
6	2.0V
7	2.0V
8	Ground

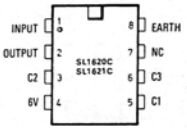




SL620C/21C @ +6V supply

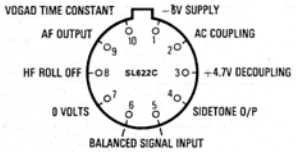
Pin	Voltage
1	1.2V
2	Output – varies with input
3	Varies with input – max. approx. 3V
4	Supply
5	Varies with input – max. approx. 3V
6	Varies with input – max. approx. 5V
7	N/C
8	Ground

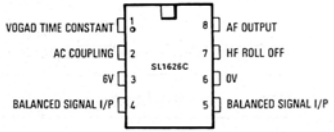




SL622C & SL1626C @ +6V supply and 18mV rms

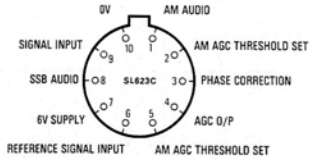
Pin	Voltages	
	SL622C	SL1626C
1	Supply	1.6V
2	2.0V	2.8V
3	4.8V	Supply
4	3.6V	1.0V
5	0.85V	1.0V
6	0.85V	Ground
7	Ground	1.3V
8	1.3V	1.3V
9	1.3V	
10	1.6V	





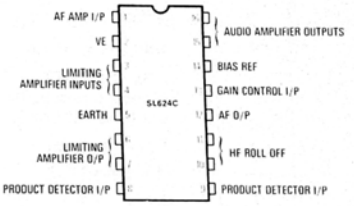
SL623C

Pin	Voltage
1	0.9V
2	0.9V
3	0.9V
4	Varies
5	0.7V
6	3.0V
7	+6V
8	3.9V
9	1.4V
10	0V



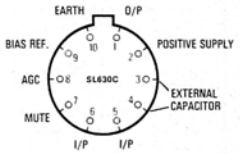
SL624C @ +12V supply

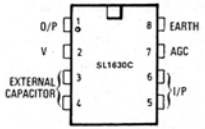
Pin	Voltage
1	1.7V
2	Supply
3	3.7V
4	3.7V
5	Ground
6	3.7V
7	3.7V
8	5.2V
9	5.2V
10	8.3V
11	8.2V
12	9.4V to 12V
13	Gain control
14	1.2V
15	6.2V
16	6.8V



SL630C/1630C

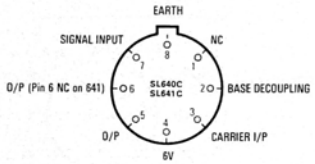
Pin	Voltage
1	3.0V
2	Supply
3	4.5V
4	1.4V
5	2.0V
6	2.0V
7 (–)	0.7V
8 (7)	0.7V (if open circuit)
9 (–)	0.65V
10 (8)	Ground

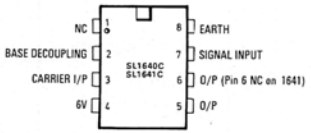




SL640C, SL641C, SL1640C & SL1641C

Pin	Voltage
1	Ground
2	2.75V
3	2.75V
4	Supply
5	5.3V (SL640C) Open collector, must go to positive supply via load (SL641C)
6	4.8V (SL640C) N/C (SL641C)
7	2.75V
8	Ground

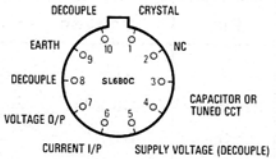


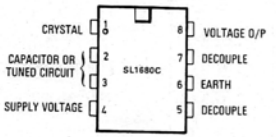


SL680C/1680C

Pin	Voltages	
	SL680C	SL1680C
1	3.5V	3.5V
2		4.2V
3	4.2V	0.75V
4	0.75V	+9V supply
5	+9V supply	1.0V
6	As pin 5*	1.5V
7	1.0V	0V
8	1.5V	1.5V
9	0V	
10	1.5V	

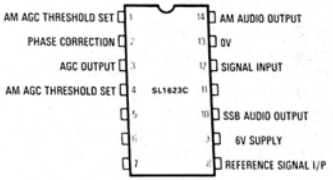
*Less with resistive load.





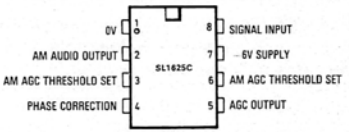
SL1623C

Pin	Voltage
1	0.9V
2	0.9V
3	Varies
4	0.7V
8	3.0V
9	+6V
10	3.9V
12	1.4V
13	0V
14	0.9V



SL1625C

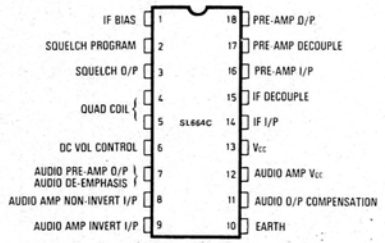
Pin	Voltage
1	0V
2	0.9V
3	0.9V
4	0.9V
5	Varies
6	0.7V
7	+6V
8	1.4V

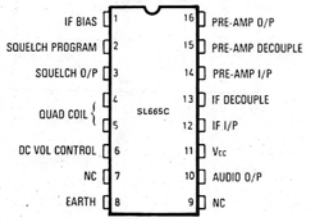


SL664C & SL665C

Pin	Voltage (SL664C)	Pin	Voltage (SL665C)
1	5.2V	1	5.2V
2	5.3V	2	5.3V
3	5.3V(0.6V)	3	5.3V(0.6V)
4	4.7V(4.2V)	4	4.2V
5	4.7V(4.2V)	5	4.2V
6	5.9V	6	5.9V
7	0.0V(1.5V)	7	
8	3.0V(2.8V)	8	0V
9	3.6V(3.0V)	9	N/C
10	0V	10	5.5V(5.0V)
11	3.0V	11	6.0V
12	6.0V	12	5.2V
13	6.0V	13	5.2V
14	5.2V	14	1.7V
15	5.2V	15	1.7V
16	1.7V	16	1.7V
17	1.7V		
18	1.7V		

This table gives the pin voltages on the SL664 and SL665 in both squelched and unsquelched (in brackets) conditions. Where the voltages are effectively the same only one value is given.





Appendix B

Low noise basics

INTRODUCTION

Noise performance of bipolar transistors is generally considered to be something of a black art, only understood by a few specialists and not a subject with which the average semiconductor man need concern himself. However, we all need at least a basic knowledge of noise theory. The important characteristics of the noise in bipolar devices is well understood and not difficult for anyone with basic circuit background to assimilate. As in any specialist field, jargon abounds; so in the description that follows, an attempt has been made to highlight the jargon and explain it.

NOISE AND FREQUENCY

The most important noise generators in a transistor produce *white noise.* That is noise in which the noise power in a fixed bandwidth (say, 1Hz) is independent of frequency. So, if a white noise source is being examined and a 1Hz filter is swept across the spectrum, the reading of a power meter will be constant. This means that there is as much noise power from a white noise source between 1Hz and 2Hz as there is between 1MHz and 1.000001MHz.

From this fact we can see that the noise power from a white noise source is proportional to bandwidth because each 1Hz interval will contribute an equal amount of power (and power can be added directly) so the noise power in a 1MHz bandwidth must be one million times greater than that in a 1Hz bandwidth. Now consider noise voltage which is, of course, proportional to the square root of power ($P = V^2/R$).

Noise voltage in a given bandwidth therefore varies as the square root of the bandwidth. Hence the units for *noise voltage* are normally $nV/\sqrt{Hz}$. Suppose we start with 1Hz filter on our white noise source and measure the noise voltage with a true RMS voltmeter; if the bandwidth is increased to 100Hz the noise voltage will increase by ten times and if a 1MHz filter is used then 1000 times the noise voltage will be recorded. If we take a circuit with a specified input noise of $0.8nV/\sqrt{Hz}$ typ. then in a 10kHz bandwidth the input noise voltage will be 80nV and in a 1MHz bandwidth it will be 0.8 microvolt.

The noise from an ideal resistor is also white. There is a standard equation for the noise voltage produced by a resistor

$$en_{nr}^2 = 4kTBR$$

where
- k is Boltzmans constant (1.38×10^{-23} Joules/°K)
- T is absolute temperature
- B is bandwidth (Hz)
- R is resistor value in ohms

Note that the noise depends on B, as we would expect for white noise. The dependence of e_{nr} on absolute temperature is typical of most noise generators, and the noise in transistors shows a similar dependence. Resistor noise of this type is commonly referred to as *thermal noise* or *Johnson noise*. These names mean just the white noise produced by a resistor and are completely interchangeable.

Another example of white noise is *shot noise*. This is produced when a current flows through a conductor and represents the random nature of the current flow. No attempt will be made in this note to distinguish between thermal and shot noise, since they are both white. The distinction is only important when noise equations are being derived from basic transistor models. As far as the user of an amplifier is concerned, the distinction is irrelevant.

Two other types of noise also exist which affect the noise spectrum at low and high frequencies – low frequency noise and high frequency noise.

Low frequency noise

One type of low frequency noise is commonly referred to as 1/*f noise* or *flicker noise*, and is not white. The noise power in a given bandwidth is inversely proportional to frequency. In a 1Hz bandwidth, say 9 to 10Hz, the noise power will be ten times greater than in a 1Hz bandwidth about 100Hz, and one hundred times greater than at 1kHz.1/*f* noise is specified either by a narrow band low frequency noise measurement or more usually, by the *flicker* (or 1/*f*) *noise knee*. This is the frequency at which the noise power starts to rise. At frequencies above the knee the dominant noise is white and at frequencies below the knee it follows a 1/*f* law.

Another type of low frequency noise is *popcorn noise* or *burst noise*. This does not in general have a 1/*f* frequency spectrum and is visible on a scope as a series of random square waves. This sort of noise used to be a problem particularly with op. amps but modern processes tend to be immune and Plessey Process III has the reputation of being almost completely free of popcorn noise.

High frequency noise

This is not important for IC amplifiers because usually the gain falls off before the noise rises. However, at frequencies approaching the f_T of the transistors then the noise increases. This is important in microwave amplifier design.

Figure 1 shows a typical transistor noise v. frequency plot. *Flicker* (1/*f*) and high frequency noise will not be discussed further but we will concentrate on the important region where the noise is white.

Equivalent input noise voltage

In order to simplify noise calculations on the overall system, it is normal to refer all noise generators back to the input. This means that the system can be analysed as an ideal noiseless system with a noise generator equal to the *equivalent input noise voltage* connected to the input. A low noise video amplifier can be considered to be an ideal noiseless amplifier with a 0.8 nV/$\sqrt{}$Hz white noise generator connected to its input. This seems nice and simple until it is realised that the equivalent input noise voltage generator is not constant but varies with source impedance.

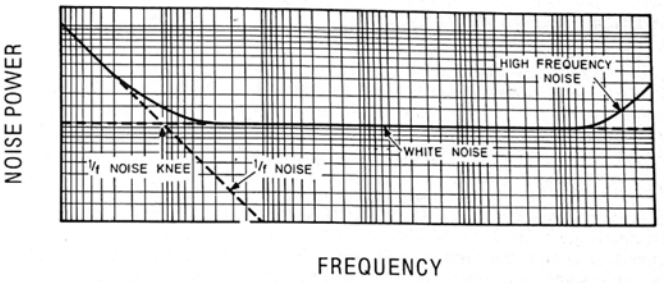


Fig. 1

Let us ignore this effect for the moment and calculate the output noise voltage that would be expected from the amplifier with an ideal 50 ohms resistor connected to its input. This involves calculating the noise generated by the resistor, adding the amplifier noise and multiplying this by the gain of the amplifier. Since the noise generated by the resistor and amplifier are both random the combined effect is obtained by adding the squares and then taking the square root.

Equivalent input noise voltage of amplifier	0.8nV/$\sqrt{}$Hz
Noise voltage produced by resistor at 25°C (from standard formula 4k TBR)	0.7nV/$\sqrt{}$Hz
Combined input noise voltage	1.06nV/$\sqrt{}$Hz
Output noise voltage (Gain = 60 dB)	1.06uV/$\sqrt{}$Hz
Output noise voltage in 6MHz bandwidth	1.06x$\sqrt{}$6,000,000
=	2.6 mV

Thus the RMS value of the noise measured on the output of the amplifier would be 2.6mV. It is most important to realise that the quivalent input noise voltage given in specifications is just for the amplifier and does not include the noise produced by the source.

IMPORTANT POINTS SO FAR

1 For white noise the noise power in a fixed bandwidth is independent of frequency.

2 The important noise sources in a bipolar transistor are white.

3 A noisy amplifier can conveniently be represented as an ideal noiseless amplifier with a noise generator connected to its input.

4 The magnitude of this generator is defined as the equivalent input noise voltage of the amplifier.

5 In the real world extra noise will be present at the input associated with the source itself.

SOURCE IMPEDANCE

The model we have used so far for noisy amplifier works quite satisfactorily as long as the variations in the equivalent input noise voltage of the amplifier with source impedance are taken into account. A slightly more complicated model can be used in which the amplifier noise generators depend only on the amplifier and do not vary with the source impedance. This is clearly better. The amplifier does not change if the source is changed so why should the equivalent input noise?

The incorrect assumption which has led to this problem is that the amplifier noise can be represented just by a voltage generator. If we assume there are two noise generators on the input to the amplifier, a voltage generator and a current generator, then the magnitudes of these depend only on the amplifier. The equivalent input noise voltage we have used so far represents the combined effect of these two. The two generators are:

1 Input noise voltage e_n (nV/$\sqrt{}$Hz)

2 Input noise current i_n (pA/$\sqrt{}$Hz)

The equivalent input noise voltage e_{na} is given by

$$e_{na}^2 = e_n^2 + R_s^2 i_n^2$$

where R_s is the source impedance.

The total voltage is therefore given by adding the voltage generated by i_n flowing in R_s to the voltage generator where the addition is made by the normal sum of squares method. For a typical low noise video amplifier

$$e_n = 0.8\text{nV}/\sqrt{\text{Hz}}$$

$$i_n = 1.7\text{pA}/\sqrt{\text{Hz}}$$

These are constant for any particular amplifier and the variation of e_{na} with source impedance is given by the presence of R_s in the equation for e_{na} given above. At low source impedance the voltage generator dominates and $e_{na} = e_n$ whilst at high values of source impedance the current noise term dominates and $e_{na} = R_s i_n$. This is illustrated in Figure 2.

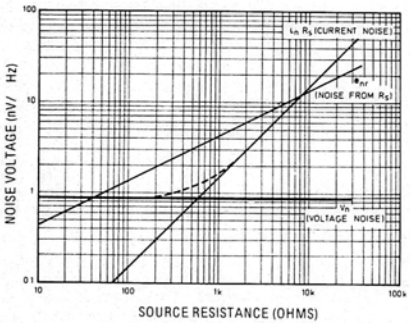


Fig. 2

The generators e_n and i_n can be changed by varying the transistor geometry to its operating current but decreasing the one tends to increase the other so the art of designing low noise amplifiers is to get the best compromise to suit the source impedance specified.

NOISE FIGURE ETC.

So far, we have been taking equivalent input noise voltage as the measure of amplifier quality. This is unrealistic in many cases since really what is required is that the amplifier should contribute significantly less noise than that introduced by the source itself. A reasonable source to consider is an ideal resistor at room temperature. As mentioned previously the noise voltage produced by such a resistor (e_{nr}) is given by

$$e_{nr} = 4\text{kTBR V}/\sqrt{\text{Hz}}$$

This is also plotted on Figure 2.

Noise figure compares the amplifier noise with that from the source and produces a figure of merit. The exact definition is that *noise figure* is

$$(e_{nr}^2 + e_{na}^2)/e_{nr}^2$$

The top of this ratio is just the square of total noise present at the input, taking into account the noise from the source; this is divided by the square of the noise voltage produced by the source itself. The noise figure of the SL1205 can be derived from Figure 2, since e_{nr} and e_{na} are both shown. This is plotted in Figure 3.

At low source impedances the noise figure rises although the noise voltage is flat because the bottom of the expression for noise figure is falling as the noise voltage from the source reduces.

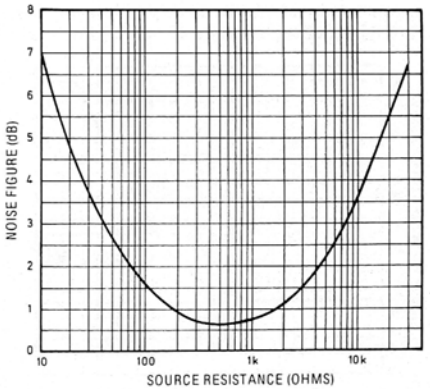


Fig. 3

Noise figure is normally expressed in dB — an ideal noiseless amplifier having a noise figure of 0 dB. One of the reasons why noise figure is widely used is that it is not bandwidth-dependent. It represents the ratio of two squared noise voltages which, as long as they are measured in the same bandwidth and the noise is white, does not depend on what particular bandwidth was used.

A distinction is sometimes drawn between *spot noise* and *wideband noise*. Spot noise simply means that the measurement bandwidth is small compared with the centre frequency. For white noise, the spot noise figure will be the same as the wideband noise figure. If the wideband noise figure is larger then the measurement bandwidth must include either 1/*f* or high frequency noise components.

The problem with noise figure is that the amplifier noise is compared with that from a resistor at room temperature. This is alright if this is a reasonable representation of the actual source but it is not uncommon for sources to be much noisier or much quiter than their resistance value would suggest.

An example of a noisy source is a photoconductive infra red detector in which the bias current contributes excess noise. If a source is cooled below room temperature it will be less noisy and an example of this is a cooled photovoltaic detector in which there is no bias current and the only noise contribution is the noise from the slope resistance at 77°K.

Another fairly common measure of amplifier noise is Equivalent Noise Resistance or NER. This is simply derived from e_{na}, the equivalent input noise voltage. NER is the value of ideal resistor that would generate a noise voltage equal to e_{na}. This can also be derived from Figure 2 and NER is plotted in Figure 4.

At low values of source impedance where the voltage noise generator is dominant NER can be related to real resistors in the transistor

$$NER = r_{bb} + r_e/2$$

But when the current noise starts to dominate this equivalence is invalid and, in fact, $NER = R_s^2/2r_e$ at high values of source impedance.

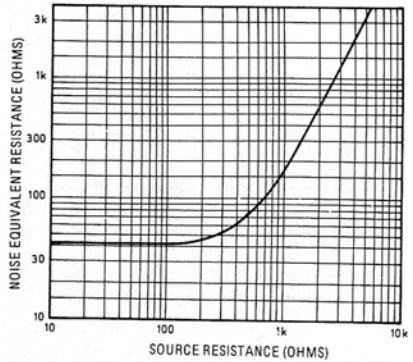


Fig. 4

SUMMARY

1 For more realistic representation of the equivalent input noise of a bipolar stage current and voltage noise generators must be used.

2 At low values of source impedance the voltage noise generator dominates and the noise voltage is constant.

3 At high values of source impedance the current noise generator dominates and the noise voltage increases steadily as R_S is increased.

4 Noise Figure is a figure of merit which compares the amplifier noise with that from an ideal resistor at room temperature.

5 It is meaningless to specify noise figure or equivalent input noise voltage without also specifying source impedance.

DEFINITIONS

e_{no}	Total output noise voltage
e_{na}	Equivalent input noise voltage in 1Hz bandwidth
e_n	Magnitude of voltage noise generator in 1Hz bandwidth
i_n	Magnitude of current noise generator in 1Hz bandwidth
e_{nr}	Noise voltage from an ideal resistor in 1Hz bandwidth
k	Boltzmann's constant ($1{,}38 \times 10^{-23}$ Joules/°k)
T	Absolute temperature
B	Bandwidth (Hz)
NF	Noise Figure (dB)
NER	Equivalent Noise Resistance
R_s	Source resistance
G	Amplifier voltage gain

$e_{na}^2 = e_n^2 + R_s^2 i_n^2$
$e_{nr}^2 = 4kTBR$
$NF = 10 \log (1 + e_{na}^2/e_{nr}^2) = 10 \log (1 + NER/R_s)$
$NER = e_{na}^2/4kT$
$NER = r_{bb} + r_e^2/2 + R_s^2/2r_e$
$e_n^2 = 4kT (r_{bb} + r_e/2)$
$i_n^2 = 2kT/r_e$
$e_{no}^2 = BG^2 (e_{na}^2 + e_{nr}^2)$

Appendix C

Characteristics and interfacing for the SP8000 series high speed dividers

INTRODUCTION

The SP8000 series of high frequency dividers achieve their characteristics of high operating frequency (extending beyond 1GHz for some of the range) and low power from the use of emitter coupled switching circuits. The dividers themselves are all built from the basic 'divide by 2' circuit shown in Figure 1. The divide by 2 circuit is a master-slave arrangement, and has a very flexible set of design constraints.

Perhaps the most significant of these is the size of the tail current supplying each differential pair. The different characteristics of devices in the SP8000 series are achieved by variation of this parameter. For example, the SP8667, a 1.2GHz decade, operates with a tail current in the first stage of 6mA giving a typical current consumption of 80mA for the four divide by 2 stages comprising the decade whereas the SP8655, a 100MHz divide by 32, operates with a tail current of 350 microamps giving a typical current consumption of only 10mA for the five divide by 2's.

Another technique employed to improve speed is that of driving the clock transistor (Ta, Tb in figure 1) directly instead of through a level shifting emitter follower. A further refinement is to use a common base stage as a collector load to reduce collector mode capacitance and this is employed on the faster types such as the SP8614, 5, 6 divide by 4 and SP8665, 6, 7 divide by 10. This does of course have the disadvantage that the power supply voltage has to be increased from the normal 5.2V to 6.8V.

This tailoring of the divider circuits means that it is not possible to treat the SP8000 series of dividers as a consistent family for interfacing purposes. The variations of the dividers are covered later in this note.

GENERAL PHYSICAL LAYOUT CONSIDERATIONS

The high performance of the SP8000 series of counters can only be exploited if the appropriate construction techniques are employed. All signal lines, both input and output, should be characterised as transmission lines and terminated correctly to avoid reflections. This is particularly important at the device input as the high input sensitivity and speed of most of the dividers makes them prone to counting reflected edges. Care must also be taken on output lines as the counters generate extremely fast edges (typically 2 ns).

The dividers are usually employed in systems which predominantly operate at much lower frequencies than the dividers themselves and so many of the precautions necessary with large scale ECL logic systems are not necessary. The most usual interconnection technique employed at high frequencies is microstrip line.

Clearly, to facilitate line terminations it is desirable that the input impedance of the dividers should be much higher than the characteristic impedance of the line. It is recommended that lines with a characteristic impedance of

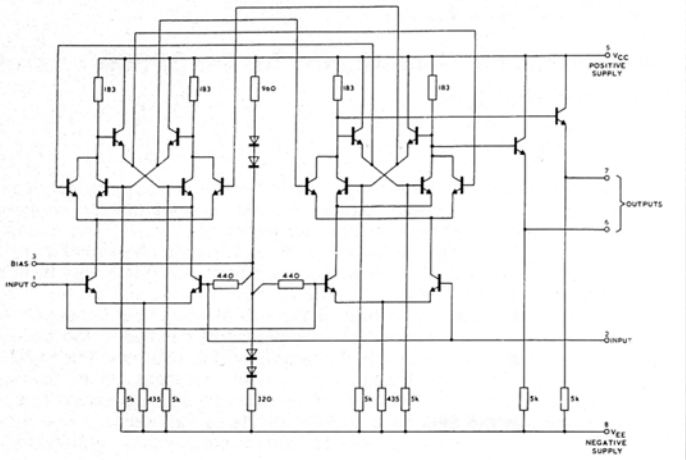


Fig. 1 Divide by 2 circuit diagram. All resistor values are nominal

50 ohms be used if possible. Higher characteristic impedances should be avoided as correct termination becomes more difficult to achieve and cross-talk and noise performance deteriorates.

In addition to these signal line restrictions the normal precautions appropriate to the frequencies and edge speeds being handled should be observed. These include the use of a ground plane (already required for the microstrip signal lines) which may be the positive supply.

The selection of the positive supply for the ground plane ensures that the poor immunity of ECL gates with respect to their positive (Vcc) supply is not a performance hazard. All components, particularly decoupling capacitors, should be of a suitable type for the frequencies involved.

If it is not desirable to have a positive ground (for example, where a predominantly TTL system employs one or two high speed dividers), then it is permissible to operate SP8000 dividers with a negative ground. However, it should be noted that output levels are referenced to the positive supply and any drift in this will be reflected in the output levels. Great care should be taken with supply decoupling, preferably decoupling every ECL package Vcc supply pin to ground so that supply noise does not cause mis-counting of a divider.

Provided that these simple precautions are observed the SP8000 dividers can be applied to a system without any problems.

INPUT INTERFACING

The high speed and sensitivity of the SP8000 series of dividers is achieved in part by omitting the level shifters normally employed in ECL counter circuits. These are replaced by input resistors which bias the clock inputs at the centre of their active region. For this reason AC coupling to the clock inputs is recommended for the majority of the dividers.

Although DC coupling to clock inputs is permissible, in practice it is not easy to provide a source which will track the input bias level sufficiently accurately to maintain the specified sensitivity. The only exceptions to this rule are the SP8600 and SP8601 divide by 4 circuits, where the inputs are not prebiased and a bias chain has to be provided externally, and the SP8640, 8641, 8642 and 8643 divide by 10/11 circuits which have an ECL III type clock input and so should be driven from an ECL III or ECL 10K gate. As no internal bias is provided for the clock inputs on SP8640 type dividers, if capacitive coupling is desired then a bias chain is required.

The technique of input prebiasing, used on most of the SP8000 dividers, which is responsible for their high sensitivity, does have one disadvantage. If Fig. 2 the graph of input sensitivity against frequency for a typical SP8630, is studied, it can be seen that the curve has a pronounced dip at around 250MHz. This is interpreted as a tendency to oscillate in the absence of any input signal. It should be emphasised that provided a signal greater than the minimum specified is present at the clock input then there is no tendency to miscount.

If the divider is being used in a continuous system such as a frequency synthesiser then clearly this is not a problem. However, in other applications, such as frequency counters, where the input would not be continuous this characteristic is clearly an embarrassment. Fortunately it is a simple matter to remove this problem. The input prebias is counteracted by adding a small bleed resistor to Vee on the clock input. The required value of this resistor varies from type to type. It is not important which clock input is offset, but a slight decrease in sensitivity is usually experienced. In almost all cases the counters will still meet the guaranteed performance specification.

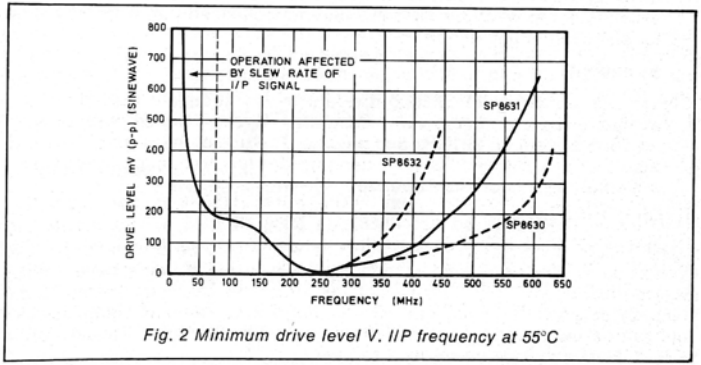


Fig. 2 Minimum drive level V. IIP frequency at 55°C

The only devices in which this characteristic is not present are:

(a) SP8601

This divide by 4 circuit has no prebias on the inputs and was originally designed to allow transformer coupling to the inputs. A resistor is added in the emitter of one clock input to introduce a small offset to prevent self clocking. The SP8601 may be driven from any ECL II type gate or divider with ECL II type outputs.

(b) SP8640, 8641, 8642, 8643

These divide by 10/11 circuits have ECL III type clock inputs with internal pulldown resistors. It should be noted that the SP8685 500MHz divide by 10/11 is designed for AC input coupling and does *not* have internal pull-down resistors.

REFERENCE BIAS AND INPUT DECOUPLING

Most of the SP8000 series of dividers are provided either with complementary clock inputs or reference bias points. To exploit their full sensitivity and frequency specification the reference bias points should be decoupled to the systems RF ground. A suitable value for this decoupling capacitor is 15–1000pF. Values greater than 1000pF should be avoided as damage may be caused to the reference bias chain when power is applied to the circuit.

Similar comments apply to the unused clock inputs of those devices which have complementary clock inputs.

EXTENDING THE FREQUENCY AND SENSITIVITY

Frequency

Obviously little can be done to improve the upper frequency limit of the dividers except to observe the construction advice given above.

The low frequency end is not a fundamental limitation though. The specified low frequency cut off is measured with a sine wave input. However, the devices are edge sensitive and so they will operate perfectly down to DC provided the edge speed that they are driven with exceeds, for most of the dividers, 100V/microsecond (i.e. 6.4ns rise time for an 800mV input signal).

Sensitivity

If the sensitivity of SP8000 dividers is not adequate then there are available several microwave integrated circuits which will provide 10–26dB of gain up to 1GHz and beyond. The use of these amplifiers and also that of input circuits for extending the low frequency limit is described at the end of this Appendix.

OUTPUT CIRCUITS

The SP8000 dividers have output circuits which may be classified into two types: open collector or emitter follower. Most of the dividers have emitter follower outputs giving ECL II type outputs, which are easily interfaced. Some of the dividers have an emitter follower output, but with a limited output swing. This can be increased by an additional external emitter load. These are the SP8602, 8603 and 8604 divide by 2 circuits.

Only three of the dividers have open collector outputs. These are the SP8600, 8601 divide by 4, the SP8634, 8635, 8636, 8637 divide by 10 and SP8655, 8657, 8659 low power dividers. The divide by 4 and divide by 10 circuits both have complementary current sources. These are designed to operate in a non-saturating mode. The low power dividers have a saturating free collector output.

Both output circuits can interface with TTL and CMOS (providing that the open collector does not go more than 12V more positive than Vee). Type 1 can also directly interface with ECL II type inputs whereas type 2 can directly drive a much higher load and is particularly useful where the ECL divider and the following TTL or CMOS operate off of the same supplies. The recommended operation of these open collector outputs is described below.

Type 1 Open Collector Output

SP8600, 8601

The output current of these devices is guaranteed to be at least 2mA. It has a small temperature coefficient and can be expected to be less than 3.5mA under all conditions. Care should be taken to prevent the output transistors saturating as this will reduce the maximum operating frequency.

SP8634, 8635, 8636, 8637

These BCD divide by 10 circuits have type 1 open collector current source outputs on the BCD outputs and on one carry output (the other carry is an ECL II type.) They have a higher operating point than those on the SP8600 and so it is not possible to use them to drive ECL gates. The BCD outputs have a limited drive capability. The carry output can drive 3 TTL loads with a lower collector load. For maximum performance it is recommended that the ECL carry output (pin 9) be used to drive a level shift circuit such as the ECL 10K type SP10125.

Type 2 Open Collector Output

SP8655, 8657, 8659

These low power dividers have a type 2 open collector output. This type of output has two advantages in low power applications. The saturating output allows the device to operate off the same supply as its following TTL or CMOS dividers and the power consumption of the output can be tailored to the particular system's power and speed requirement. The maximum DC TTL load that can be accommodated is 2 standard TTL inputs with a 2.7 kilohms pullup resistor.

Emitter Follower Outputs

All the remaining dividers in the SP8000 series have emitter follower outputs and all except the SP8602, 8603 and 8604 can be directly interfaced with ECL II by the addition of a 1.5 kilohm resistor to Vee. ECL III or 10K levels are generated by the addition of a series resistor. It should be noted that the devices are not capable of driving 50 ohm transmission lines directly. Some may however, be used to drive series terminated 50 ohm lines, provided sufficient current is maintained in the output emitter follower.

These devices, although having an emitter follower output which can drive ECL II, III or 10K via interfaces do not have sufficient drive capability for a low impedance transmission line. If operation in a transmission line environment is desired then an ECL line receiver such as the SP10116 should be used.

SUMMARY

The SP8000 series of high speed dividers represents a family of devices whose input and output characteristics present the engineer with a sufficient diversity to allow the correct solution for any system. The devices are easy to use in a system provided the constraints covered above are observed.

Appendix D

Using the SL 652 as a stable tone source and as an FSK modem

The Plessey SL652 is an integrated circuit designed for use in the FSK modem. It comprises a highly stable oscillator (which may be programmed digitally or by a variation of voltage, current or resistance) and a sensitive phase comparator. It may be used as a simple, stable tone source, as an FSK modem transmitter or as a phase-locked FSK receiver.

The SL652 is a simplified version of the Plessey SL650. Since there is a comprehensive application note available on this circuit no detailed description of the functioning of the SL652 will be given here. The block diagram, the truth table of the binary programming and the arrangement of a programmed oscillator, however, are shown in Figs. 1 to 3 respectively. It is important to remember that the oscillator stability of about ±20ppm per degree C relates only to the integrated circuit itself and if inadequate timing resistors and capacitors are used a far worse performance will result. In high stability applications, polystyrene, polycarbonate or silver mica capacitors and wirewound or metal oxide resistors should be used.

In normal use the two negative supply pins, pin I and pin II, are joined and in this case the frequency of the oscillator is 1/CR where C is the timing capacitor and R is the timing resistor (if the programming input is set to select two timing inputs, R is the value of the resistor formed by the two resistors in parallel).

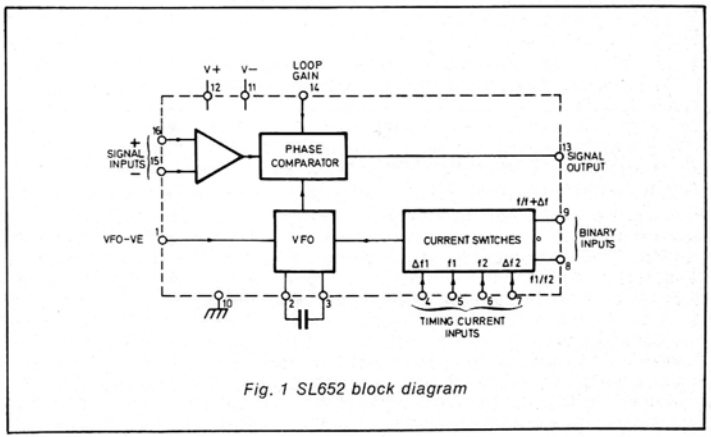


Fig. 1 SL652 block diagram

Pin 8	Pin 9	Timing Pins	VFO Frequency
LO	LO	5	$\frac{1}{CR_2}$
LO	HI	4 & 5	$\frac{1}{CR_2} + \frac{1}{CR_1}$
HI	LO	6	$\frac{1}{CR_3}$
HI	HI	6 & 7	$\frac{1}{CR_3} + \frac{1}{CR_4}$

Fig. 2 Binary interface relationships

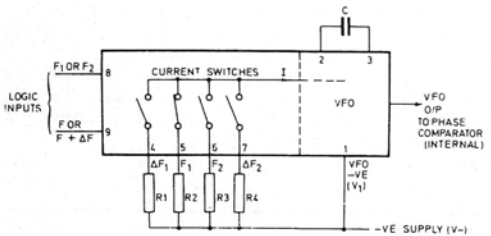


Fig. 3 VFO and binary interface

A STABLE TONE GENERATOR

The circuit diagram of a stable tone generator is given in Fig. 4. The output is a square wave of about 9V p-p. If suitably stable timing components are used the frequency stability will be well under 0.1 per cent over the range 0°C to +70°C which makes the oscillator ideal as a tone generator for repeater access in amateur 2 metre transceivers or as an access tone for any of a number of tone operated systems in commercial radio. If only one stable tone is required the programming inputs P1 and P2 may be grounded or left unconnected; if more than one tone is required the program inputs may be used to select whichever is required. If the program inputs are driven by a clock or sequencer of some sort, a tone sequence containing up to four different tones may be produced. The logic level on the program inputs are ground (or open circuit) and +3V to +6V.

If the oscillator is required only as a repeater access tone generator R1, R3 and R4 may be omitted, R2 should be 5 kilohms and C should be 0.01 microfarads. Since there will be tolerances in the circuit and both the resistor and the capacitor it is probably best to use one capacitor but to select two or three resistors (or perhaps use a preset potentiometer in series with a 51 kilohm resistor) to set the frequency accurately.

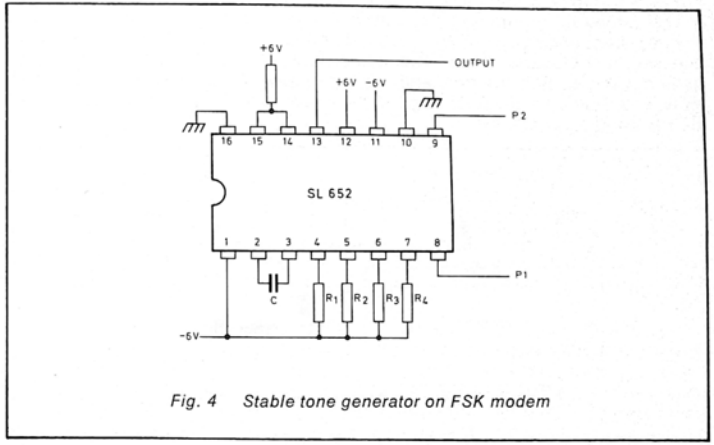


Fig. 4 Stable tone generator on FSK modem

AN FSK MODEM TRANSMITTER

An FSK modem transmitter consists of a circuit which transmits one frequency when its input is in one logical state and a different one when its input is in the other state. It is evident that the tone generator in Fig. 4 will function equally well as a modem transmitter if the datastream is applied to input P2 and resistor R2 set to give the space frequency and resistors R1 and R2 in parallel set to give the mark frequency.

If only a single carrier frequency is required R4 and R4 may be omitted and P1 grounded but if the modem is required to operate on either of two carrier frequencies one or other may be selected by P1 and R3 and R3 + R4 may be used to program 'space' and 'mark' of the other channel. Alternatively P1 may select whether the SL652 is used as a modem transmitter or as a tone burst generator.

The upper frequency limit of the SL652 VC0 is at least 100kHz so such a modem will work at carrier frequencies up to this and at up to at least 25 kilobauds. It is equally suitable for use with carriers between 750Hz and 3kHz and at speeds of around 50 bauds.

The only consideration, other than the maximum frequency of operation, is to keep the timing current within the limits of 20 microamps and 2mA which implies that the timing resistors should be more than 3 kilohms and less than 300 kilohms. The timing capacitor should not be less than 1000pF lest changes of capacitance with temperature within the integrated circuit affect the timing.

A PHASE-LOCKED LOOP FSK DEMODULATOR

Fig. 5 shows the SL652 used as a phase-locked loop demodulator. The signal input is applied to pins 15 and 16 (or if more convenient to either pin while the other is grounded) and the phase comparator output is fed back into the VC0 by a resistor, and also to a voltage comparator via a three pole filter. The output of the voltage comparator is the digital output of the demodulator.

The values of the timing components C and R_F are chosen to give a free-running frequency $f_N = 1/CR_F$ equal to the carrier frequency i.e., midway between the mark and space frequencies of the system. The feedback resistor R_F is chosen so that the frequency f_N is roughly twice the shift between the mark and space frequencies e.g., if the mark is 1850Hz and space 1650Hz then f_N should be 400Hz.

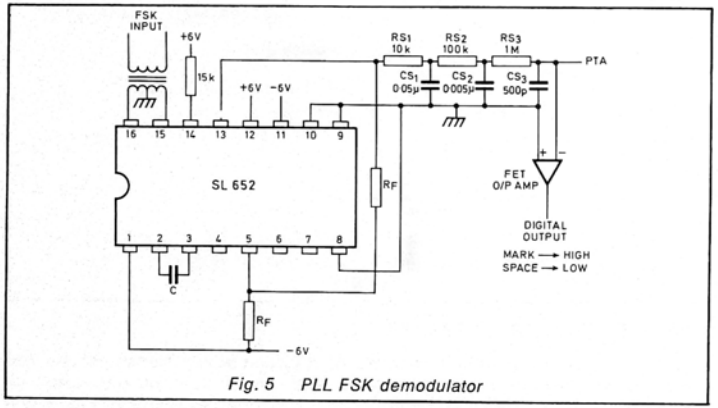


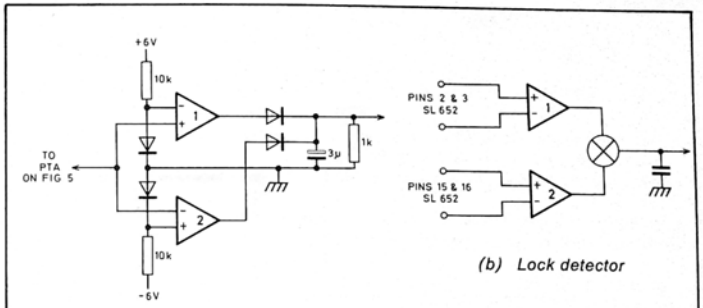
Fig. 5 PLL FSK demodulator

The filter resistors should increase in steps of ten times and the capacitors decrease in steps of ten times as shown in the diagram. The time constants RS1.CS1, RS2.CS2 and RS3.CS3 should be equal and have a value of approximately $1/f_N$.

Since RS1 must be large enough not to load the output of the phase comparator and RS3 would be a hundred times larger it is important that the voltage comparator has a high input impedance and a very low bias current – less than 10nA. An FET input operational amplifier either MOS or JFET is ideal. The offset voltage or current is less important since there should be a shift of several hundred mV or more at the amplifier input between 'mark' and 'space'. A good value for RS1 is 10 kilohms as shown.

Many modem receivers require a detector to indicate when a signal is being received – often to start a teletype or some similar function. Fig. 6 shows two ways in which this may be done. Both methods use two FET input operational amplifiers.

Fig. 6a shows a tone detector which is effectively a window detector looking at the potential at the output of the low pass filter in the demodulator. When the PLL has no signal at its input, or is receiving a tone well removed from the one



(a) Tone detector

(b) Lock detector

Fig. 6 Carrier detectors

to which it is tuned, the output of the LPF is near to ground. When a 'space' tone is received, however, it rises and when a 'mark' tone is received it falls. Amplifier 1 detects a voltage above +0.7V at its input and gives a positive output; Amplifier 2 detects a voltage below 0.7V at its input and gives a positive output. Either of these positive outputs charges the capacitor and provides a positive output from the detector. It is important that FET amplifiers be used in this, and in the next, application as normal bipolar operational amplifiers have too large a bias current.

The system in Fig. 6b is a lock detector. Amplifier 1 obtains a quadrature signal from the VC0 in the PLL and squares it. Amplifier 2 amplifies the input to the PLL. The outputs of these amplifiers are mixed in a double balanced modulator. When the PLL is not locked to signal, the product of the quadrature of its VC0 and its input signal is AC without a DC component, but when the loop is locked, although there may be a residual AC, the DC component in the output of the double balanced modulator is large and may be filtered and used to operate a switch. The sense of the output DC depends on the phase of the two signals and may be reversed by reversing the input to one of the amplifiers.

A SIMPLE FSK TRANSCEIVER

Fig. 7 shows a simple transceiver. It consists of the transmitter and the receiver described above (and using single single-ended input) combined, with some switching, to use a single SL652. The same comments apply as to the separate transmitter and receiver and the same considerations apply to the choice of components.

There is no reason why carrier detection as described above, and many other refinements, should not be added to this simple transceiver which would still be much simpler than most transmitters or receivers but have as good a performance.

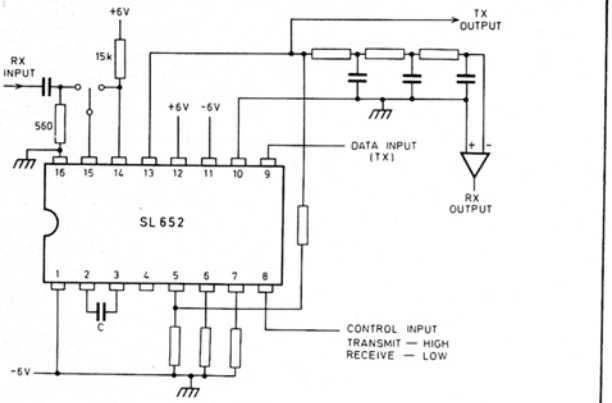


Fig. 7 Simple transceiver

There are only two points which must be remembered when using the SL652 in the systems described above, and both relate to the power supply. Neither power rail must exceed 6 volts, and the negative supply rail must not exceed the magnitude of the positive one. The first constraint is vital to the survival of the SL652 – quite a short exposure to a supply voltage of over 7.5 volts will destroy it. The second constraint affects the operation of the device but does not affect its life.

Appendix E

Input characterisation for the SP8000 series

Because of the wide frequency range of the SP8600 series emitter-coupled logic dividers, the input drive and impedance should be optimized.

The input impedance from 50MHz to 600MHz is mostly capacitive. Beyond 600MHz it becomes inductive.

To optimize the circuit to handle large overloads, small signals, and changes of input impedance versus operating frequency some suggestions are offered in Figs. 1, 2 and 3.

Where the frequency range to be used covers an impedance change of greater than three to one, as in Fig. 6, between 50MHz to 300MHz, a circuit shown in Fig. 1 could be added to the input. By using the appropriate input impedance curve and calculating the value of R & L, the total input impedance would be more constant over the required frequency range.

In the case of large overloads the circuit shown in Fig. 2 could be used.

When using this circuit there is typically a 3dB loss in sensitivity but the dynamic range would be increased from two to one to over four to one. The value of R depends on the maximum overdrive voltage and the hot carrier diodes used.

For low level inputs an SL1521 wideband amplifier could be used as a preamplifier for a divider as shown in Fig. 3.

By using the SL1521 and the SP8690 low power 200MHz divide by 10/11 divider, as shown in Fig. 3, the minimum sensitivity is reduced from 143mV RMS to 36mV RMS. Both units are self biased and require only coupling capacitors for interconnections. Also both parts operate from the same +5V supply at 145mW total power.

When using the SP8600 series it is recommended that good low inductance RF capacitors be used on all bias and power supply decoupling points.

The printed circuit board should be laid out with all input leads as short as possible, ample ground plane around the device and using other normal RF techniques.

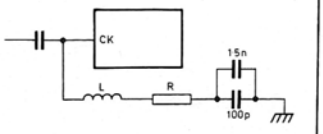


Fig. 1

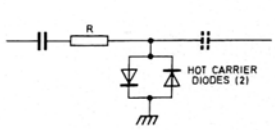


Fig. 2

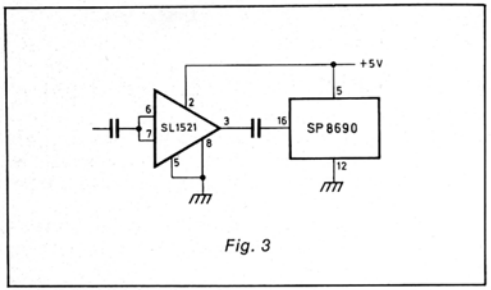


Fig. 3

SP8602, 3, 4, 7

INPUT IMPEDANCE

The input impedance is shown in Fig. 4 for the frequency range of 50MHz to 700MHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 3.1pF.

TEST CIRCUIT

The test circuit is shown in Fig. 5. All tests were made at 25°C.

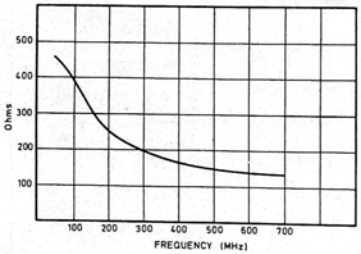


Fig. 4

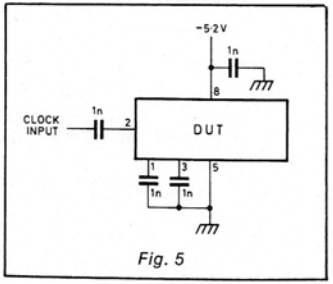


Fig. 5

SP8613, 4, 5, 6

INPUT IMPEDANCE

The input impedance is shown in Fig. 6 for the frequency range of 50MHz to 1.2GHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 4.6pF.

TEST CIRCUIT

The test circuit is shown in Fig. 7. All tests were made at 25°C.

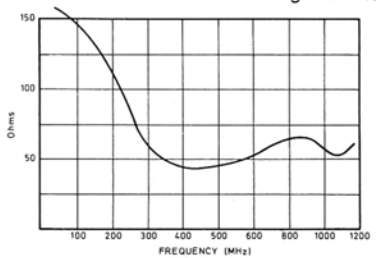


Fig. 6

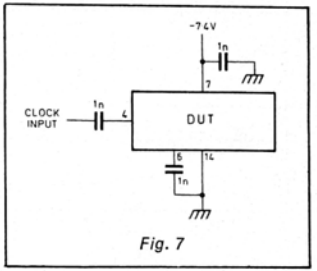


Fig. 7

SP8630, 1, 2

INPUT IMPEDANCE

The input impedance is shown in Fig. 8 for the frequency range of 50MHz to 600MHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 3.9F.

TEST CIRCUIT

The test circuit is shown in Fig. 9. All tests were made at 25°C.

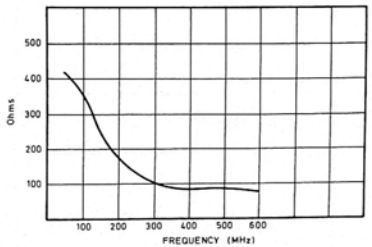


Fig. 8

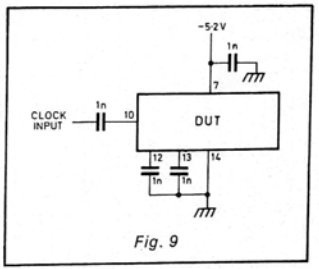


Fig. 9

SP8634, 5, 6, 7

INPUT IMPEDANCE

The input impedance is shown in Fig. 10 for the frequency range of 50MHz to 700MHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 4.1pF.

TEST CIRCUIT

The test circuit is shown in Fig. 11. All tests were made at 25°C.

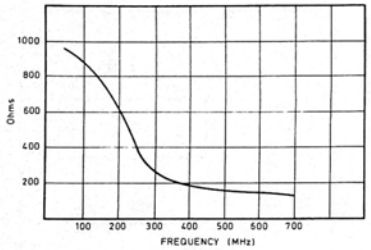


Fig. 10

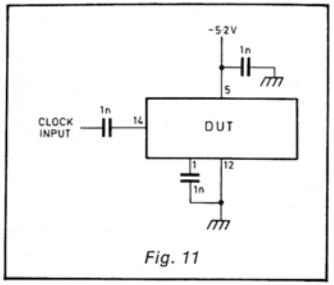


Fig. 11

SP8640, 1, 2, 4, 6, 7

INPUT IMPEDANCE

The input impedance is shown in Fig. 12 for the frequency range of 50MHz to 350MHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 2.4pF.

TEST CIRCUIT

The test circuit is shown in Fig. 13. All tests were made at 25°C.

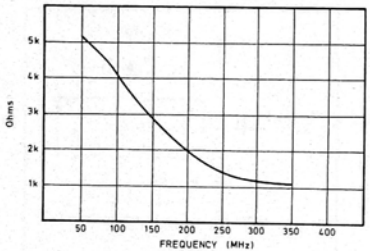


Fig. 12

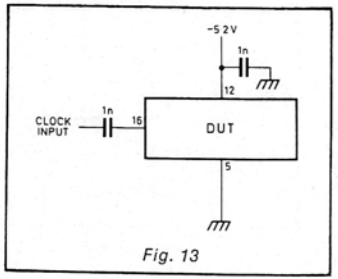


Fig. 13

SP8650, 1, 2,

INPUT IMPEDANCE

The input impedance is shown in Fig. 14 for the frequency range of 50MHz to 600MHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 6.0pF.

TEST CIRCUIT

The test circuit is shown in Fig. 15. All tests were made at 25°C.

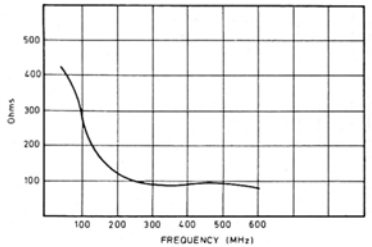


Fig. 14

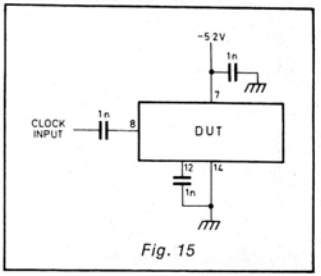


Fig. 15

SP8655, 7, 9

INPUT IMPEDANCE

The input impedance is shown in Fig. 16 for the frequency range of 50MHz to 100MHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 3.6pF.

TEST CIRCUIT

The test circuit is shown in Fig. 17. All tests were made at 25°C.

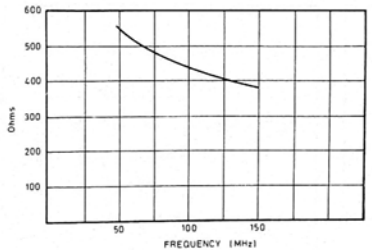


Fig. 16

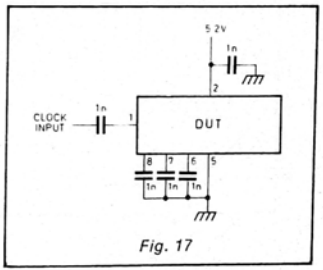


Fig. 17

SP8665, 6, 7

INPUT IMPEDANCE

The input impedance is shown in Fig. 18 for the frequency range of 50MHz to 1.2GHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 4.5pF.

TEST CIRCUIT

The test circuit is shown in Fig. 19. All tests were made at 25°C.

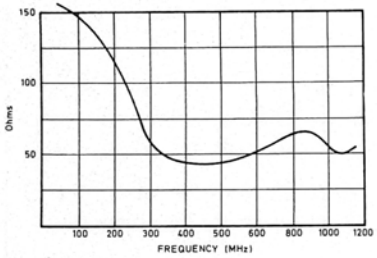


Fig. 18

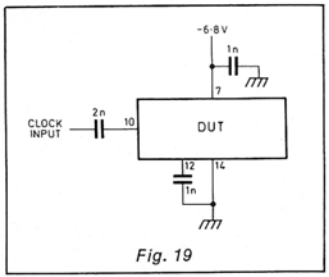


Fig. 19

SP8685

INPUT IMPEDANCE

The input impedance is shown in Fig. 20 for the frequency range of 50MHz to 500MHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 8.7pF.

TEST CIRCUIT

The test circuit is shown in Fig. 21. All tests were made at 25°C.

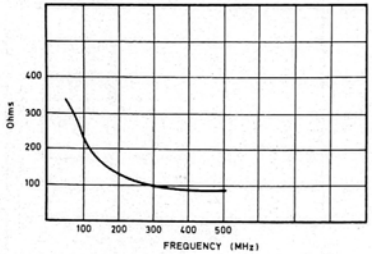


Fig. 20

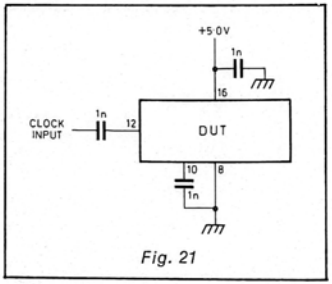


Fig. 21

SP8690

INPUT IMPEDANCE

The input impedance is shown in Fig. 22 for the frequency range of 50MHz to 200MHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 6.4pF.

TEST CIRCUIT

The test circuit is shown in Fig. 23. All tests were made at 25°C.

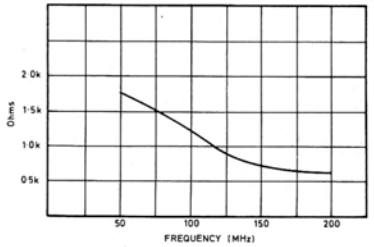


Fig. 22

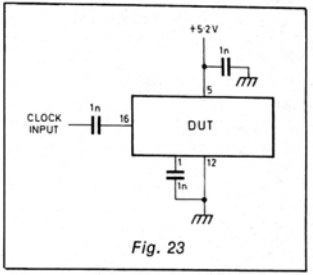


Fig. 23

Appendix F

Input characterisation for the SP8000 series
The use of hybrid IC front end amplifiers to improve the sensitivity of SP8000 series high speed dividers

The availability of low-cost hybrid amplifiers with a performance extending to 1GHz, coupled with SP8000 High Speed Dividers, allows an unparalled increase in instrument performance.

For example, using an Amperex ATF 417 as a preamplifier for an SP8616 (with a Schottky barrier diode limiter), the divider's sensitivity can be improved by at least 15dB. The circuit diagram is shown in Fig. 1. Typical room temperature performance is shown in Fig. 2, and a suitable PCB layout is given in Fig. 3.

Low end performance is limited by signal rise time requirements for the SP8616, whilst high end sensitivity is limited by the amplifier limiter performance. This can be improved by operating the ATF 417 off a higher supply. By increasing the supply to, say, +20V, a gain in sensitivity of, typically, 5dB would be expected at 1GHz.

Similar results can be obtained using the ATF 417 with other dividers such as the SP8667, 1.2GHz decade divider.

CIRCUIT DETAILS

The signal input (100MHz–1GHz) is AC-coupled to a Schottky barrier diode bridge which limits at 100mV p/p. The signal is then amplified by the hybrid A1. This combination gives about 15dB of gain with a supply of 15V. The amplifier is AC coupled, via C3, to an SP8616 ÷4 circuit (IC1). R7 provides an input offset to prevent 'no signal' oscillation. The drive capability of IC1, is increased by R8 and its output capacitively coupled to IC2 via C4 R9 provides the input offset for IC2. The output of IC2 is suitable for driving ECL II.

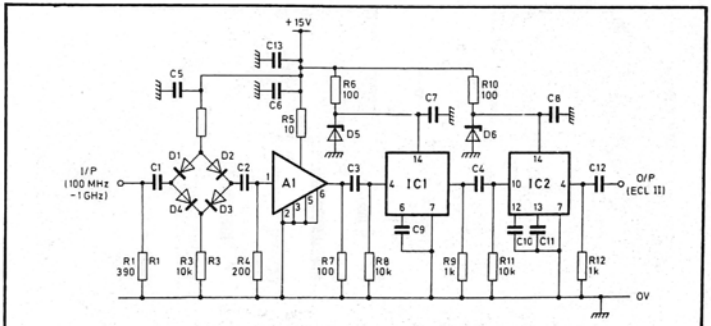


Fig. 1 UHF instrumentation ÷ 20 prescaler

COMPONENTS

D1 – D4	:	Schottky barrier diodes, HP5082–2811
A1	:	Hybrid amplifier, Amperex ATF417 or Philips OM185
IC1	:	Plessey Semiconductors SP8616B
IC2	:	Plessey Semiconductors SP8621B
D5	:	1 Watt, 7.5V Zener diode
D6	:	1 Watt, 5.1V Zener diode
R6, R10	:	100 ohms, 5 Watt, e.g. Plessey GWT-5
C1 – C12	:	1nF ceramic, e.g. ITW EMCAPS
C13	:	0.33 microfarad

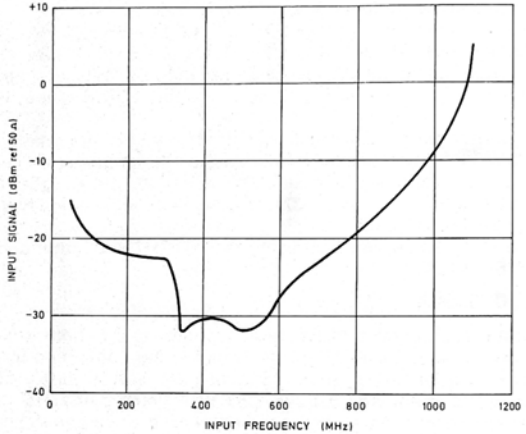


Fig. 2 Typical performance of UHF prescaler

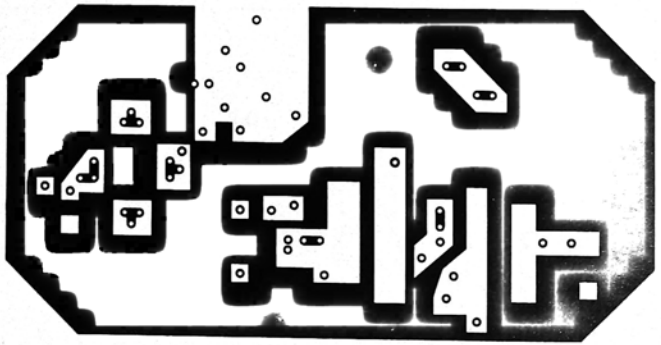


Fig. 3a Component side of board

Fig. 3b Solder side of board

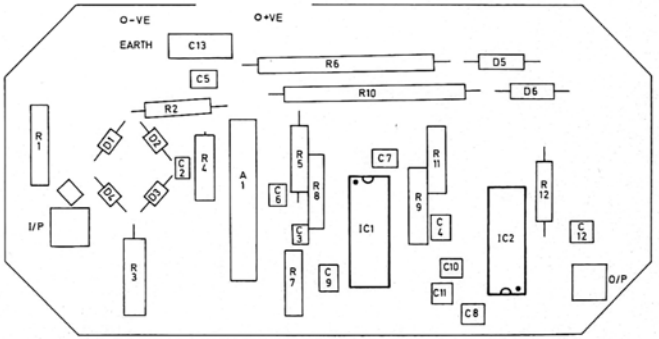


Fig. 3c Component location

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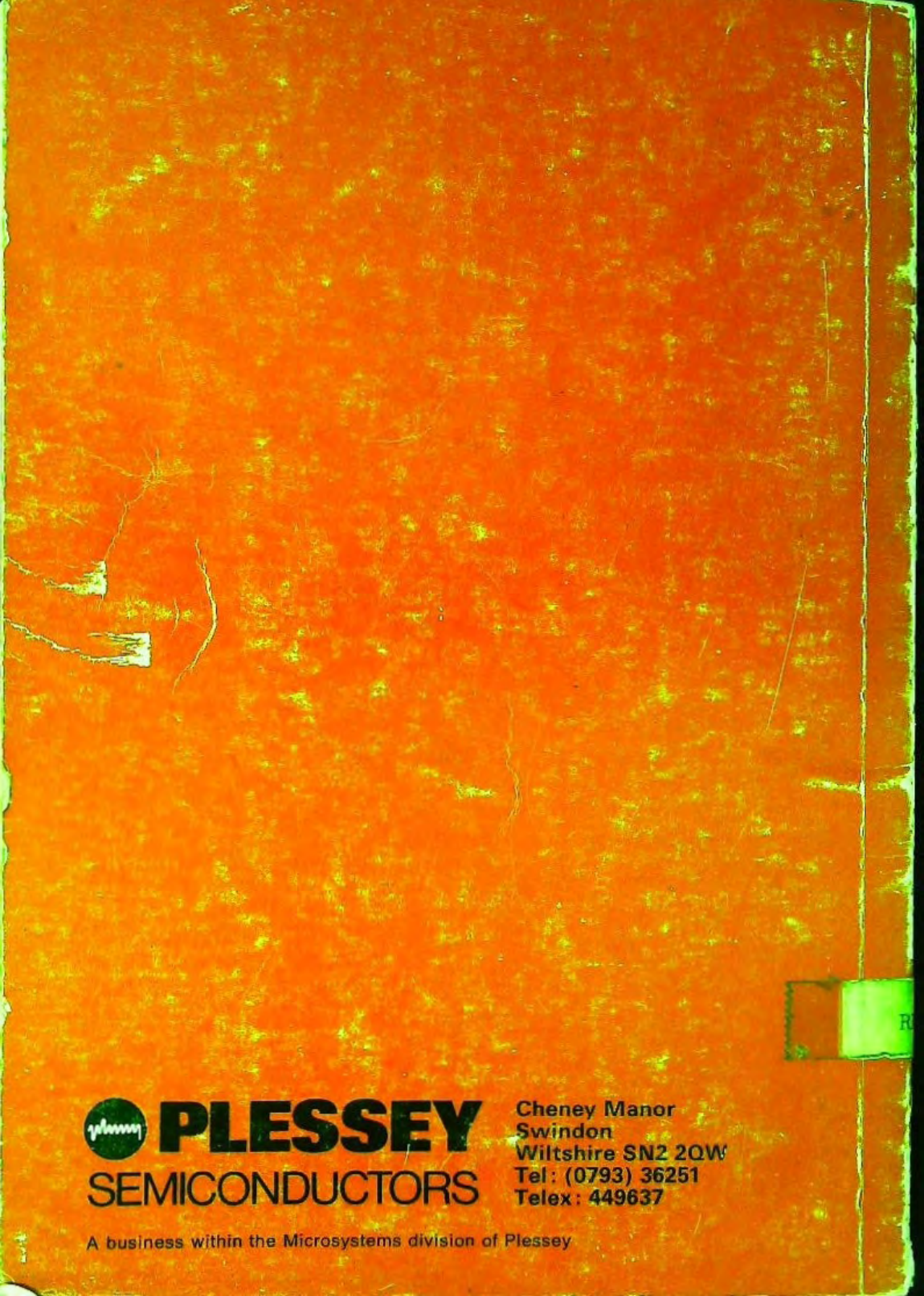

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